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October 30, 1998

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Attorney Docket Number: 501.36642X00

Sir:

Attached please find the application papers of Takahiro FUJIOKA, Kazunari KUROKAWA, Hiroshi KATAYANAGI, Mitsuru GOTO, Yukihide ODE, Akira OGURA, Kentaro AGATA, covering new and useful improvements in LIQUID CRYSTAL DISPLAY DEVICE, comprising:

Specification, Twelve (12) Claims and Abstract of the Disclosure (77 pages)

English language, Combined Declaration and Power of Attorney (2 pages)

Twenty-three (23) Sheets of Drawings Showing Figures 1-9, 10A-10E, 11A-11E, 12-22, 23A-23E, 24, 25A-25B, 26A-26B, 27A-27B, 28-30

Assignment and Recording of Assignment Letter

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Letter Claiming Right of Priority and Certified Copy of Japanese Patent Application No. 09-298227

Please charge any shortages in the fees or credit any overpayments thereof the deposit account of Antonelli, Terry, Stout & Kraus, LLP Account No. 01-2135 (501.36642X00).

Respectfully submitted,

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LIQUID CRYSTAL DISPLAY DEVICE

Background of the Invention

The present invention relates to a semiconductor integrated circuit and a liquid crystal display, particularly to an art to be effectively applied to a picture signal line driving circuit (drain driver) of a liquid crystal display capable of displaying many gradations.

An active-matrix liquid crystal display having an active element (e.g. thin film transistor) for each pixel and switching the active element is widely used as a display of a notebook-type personal computer and the like.

Because the active-matrix liquid crystal display applies a picture signal voltage (gradation voltage corresponding to display data: hereinafter referred to as gradation voltage) to a pixel electrode through an active element, there is no crosstalk generate between pixels, it is unnecessary to use a specific driving method for preventing crosstalk like a simple matrix liquid crystal display, and it is possible to display many gradations.

As the active-matrix liquid crystal display, the following are known: a TFT(Thin Film Transistor)-type liquid crystal display panel (TFT-LCD) and a TFT-type liquid crystal display module provided with a drain driver set to the upper side of a liquid crystal display panel, a gate driver set to the lateral of the liquid crystal display panel, and an interface section.

In general, when the same voltage level(DC voltage) is applied to a liquid crystal layer for a long time, the inclination of the liquid crystal layer is fixed, resultantly causing the afterimage phenomenon to shorten the service life of the liquid crystal layer.

To prevent the phenomenon, in the case of the TFT-type liquid crystal module, the voltage to be applied to a liquid crystal layer is changed to an AC voltage every certain period, that is, the voltage to be applied to a pixel electrode is changed to a positive voltage and a negative voltage every certain period in accordance with the voltage to be applied to a common electrode.

To apply an AC voltage to the liquid crystal layer, the following two methods are known: the common symmetry method and the common inversion method. The common inversion method is a method of alternately changing the voltage to be applied to a common electrode and the voltage to be applied to a pixel electrode to a positive voltage and a negative voltage. Moreover, the common symmetry method is a method of keeping the voltage to be applied to a common electrode constant and alternately changing the voltage to be applied to a pixel electrode to a positive voltage and a negative voltage in accordance with the voltage to be applied to the common electrode.

According to the common symmetry method, it is possible to

use the dot inversion method or V-line inversion method superior in small power consumption and display quality.

The above art is disclosed in US Patent Application No. 08/826973.

In the case of the dot inversion method, as shown in Fig. 30, the gradation voltage (VDH) to be applied to the odd-number-th drain signal line (D) and the gradation voltage (VDL) to be applied to the even-number-th drain signal line (D) have a polarity opposite to that of the driving voltage (VCOM) to be applied to a common electrode. That is, when the gradation voltage (VDH) to be applied to the odd-number-th drain signal line (D) has the positive polarity (or negative polarity), the gradation voltage (VDL) to be applied to the even-number-th drain signal line (D) has the negative polarity (or positive polarity). Moreover, the polarity is inverted for each line and the polarity for each line is inverted for each frame.

In this case, Fig. 30 is an illustration showing the relation between the gradation voltage to be applied to a drain signal line (D), that is, the voltage to be applied to a pixel electrode and the driving voltage (VCOM) to be applied to a common electrode. Moreover, in Fig. 4, the gradation voltage to be applied to a drain signal line (D) shows a gradation voltage when displaying black on the display screen of a liquid crystal display panel.

Thus, the dot inversion method has a disadvantage that the

chip size of a drain driver increases because a circuit for generating positive- and negative-polarity gradation voltages is necessary for each drain signal line (D).

To settle the above disadvantage, in the case of the TFT-type liquid crystal display module disclosed in the official gazette (US Patent Application No. 08/826973), the chip size of a drain driver is decreased by using the fact that the polarity of the gradation voltage (VDH) to be outputted to the odd-number-th drain signal line (D) is always opposite to that of the gradation voltage (VDL) to be outputted to the even-number-th drain signal line (D) in the case of the dot inversion method, sharing a circuit for generating positive- and negative-polarity gradation voltages by two drain signal lines (D), thereby switching the circuit by a switching section and resulting in reduction of chip size.

However, the TFT-type liquid crystal display module disclosed in the official gazette (US Patent Application No. 08/826973) has a problem that a transistor having higher withstand voltage between source and drain is necessary as the switching transistor of the switching section, thereby increasing the chip size of a drain driver when it is necessary to raise the gradation voltages (VDH and VDL) to be applied to a drain signal line (D) compared to those of a conventional TFT-type liquid crystal display module due to change of materials of a liquid crystal layer.

In the case of a liquid crystal display such as a TFT-type liquid crystal display module, a display screen is further increased in size and the display screen size tends to increase. Moreover, to eliminate an unnecessary space and improve the fine view of a display, it is requested to decrease the region other than the display region of a liquid crystal display, that is, minimize the frame portion (frame minimization).

However, when the chip size of a semiconductor integrated circuit (IC chip) constituting the drain driver increases by using a transistor having higher withstand voltage between source and drain as the switching transistor of the switching section, a problem occurs that it is impossible to deal with the frame minimization.

The present invention is made to solve the above problems of the prior art and its object is to provide an art for making it possible to put a transistor with low with stand voltage to use for a semiconductor integrated circuit as the switching element of a switching circuit in which a voltage higher than the withstand voltage between the source and drain of the transistor with low withstand voltage is applied between input and output terminals.

It is another object of the present invention to provide an art making it possible to put a transistor with low withstand voltage to use for a liquid crystal display as the switching element of a switching section in which a voltage higher than the

withstand voltage between the source and the drain of the transistor with low withstand voltage and output positive- and negative-polarity picture signal voltages to a pair of picture signal lines without increasing the chip size of picture signal line driving means.

The above objects and novel features of the present invention will become more apparent by the present specification and the accompanying drawings.

Summary of the Invention

The outline of typical one of the inventions disclosed in the present application is briefly described below.

A liquid crystal display provided with a liquid crystal display panel and a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel, wherein the picture signal driving circuit has:

a switching circuit constituted by connecting in series a first transistor in which a control voltage is applied to a gate electrode and a second transistor in which a bias voltage is applied to a gate electrode.

A liquid crystal display provided with a liquid crystal display panel and a picture signal driving circuit for supplying a picture signal voltage to the liquid crystal display panel, wherein the picture signal driving circuit has:

a first input terminal, a second input terminal, and a common output terminal,

a first switching element connected between the first input terminal and the common output terminal, and

a second switching element connected between the second input terminal and the common output terminal, and moreover wherein

the first and the second switching elements respectively include an input-terminal-side transistor in which a control voltage is applied to a gate electrode connected in series with an output-terminal-side transistor in which a bias voltage is applied to a gate electrode.

A liquid crystal display constituted with a liquid crystal display panel and a picture signal driving circuit for supplying a picture signal voltage to the liquid crystal display panel, wherein the picture signal driving circuit has:

a first output circuit for outputting a positive-polarity picture signal voltage,

a second output circuit for outputting a negative-polarity picture signal voltage, and

a switching circuit for outputting the positive-polarity picture signal voltage received from the first output circuit and the negative-polarity picture signal voltage received from the second output circuit by switching the voltages to a pair of picture signal lines, and moreover wherein the switching circuit has:

a first switching element connected between the first

output circuit and the first picture signal line of a pair of picture signal lines,

a third switching element connected between the first output circuit and the second picture signal line of a pair of picture signal lines,

a second switching element connected between the second output circuit and the second picture signal line, and

a fourth switching element connected between the second output circuit and the first picture signal line, and moreover the switching circuit

outputs the positive-polarity picture signal voltage received from the first output circuit to the first picture signal line or the second picture signal line by selectively turning on/off the first switching element, the second switching element, the third switching element, and the fourth switching element, and

selectively outputs the negative-polarity picture signal voltage received from the second output circuit to the second picture signal line or the first picture signal line.

The switching elements are constituted by connecting an output-circuit-side transistor in which a control voltage is applied to a gate electrode in series with a picture-signal-line-side transistor in which a constant bias voltage is applied to a gate electrode.

Brief Description of the Drawings

Figure 1 is a block diagram showing a schematic structure of the TFT-type liquid crystal display module of an embodiment of the present invention;

Figure 2 is an illustration showing the equivalent circuit of an example of the liquid crystal display panel shown in Fig. 1;

Figure 3 is an illustration showing the equivalent circuit of another example of the liquid crystal display panel shown in Fig. 1;

Figure 4 is an illustration showing the equivalent circuit of still another example of the liquid crystal display panel shown in Fig. 1;

Figure 5 is a block diagram showing a schematic structure of an example of the drain driver shown in Fig. 1;

Figure 6 is a block diagram for explaining the structure of the drain driver shown in Fig. 5, centering around the structure of an output circuit;

Figure 7 is a circuit diagram showing the structure of a switching circuit of the switching section of a conventional example;

Figure 8 is a circuit diagram showing the structure of a switching circuit of the switching section of an embodiment of the present invention;

Figure 9 is a sectional view of essential portions showing the sectional structures of the PMOS transistors (PM1 and PM21)

and the NMOS transistors (NM2 and NM22) shown in Fig. 8;

Figures 10(a) to 10(e) are sectional views of essential potions for explaining the outline of fabrication steps of the PMOS transistors (PM1 and PM21) and the NMOS transistors (NM2 and NM22) shown in Fig. 8;

Figures 11(a) to 11(e) are sectional views of essential portions for explaining the outline of fabrication steps of the PMOS transistors (PM1 and PM2) shown in Fig. 8;

Figure 12 is a circuit diagram showing the circuit structure of an example of the high-voltage decoder circuit of an embodiment of the present invention;

Figure 13 is a circuit diagram showing an example of the structure of the second gradation-voltage generation circuit shown in Fig. 12;

Figure 14 is a circuit diagram showing the circuit structure of another example of the high-voltage decoder circuit of an embodiment of the present invention;

Figure 15 is a schematic view for explaining the gate width of a MOS transistor constituting the high-voltage decoder circuit of an embodiment of the present invention;

Figure 16 is a circuit diagram showing the circuit structure of an example of the low-voltage decoder circuit of an embodiment of the present invention;

Figure 17 is a circuit diagram showing the structure of a switching circuit of the switching section of an embodiment of

the present invention;

Figure 18 is a sectional view of essential portions of sectional structures of the PMOS transistors (PM1 and PM21 and the NMOS transistors (NM2 and NM22);

Figure 19 is a circuit diagram showing the structure of a switching circuit of the switching section (2) of an embodiment of the present invention;

Figure 20 is a sectional view of essential portions showing the sectional structures of the PMOS transistors (PM1 and PM21) and the NMOS transistors (NM2 and NM22) shown in Fig. 19;

Figure 21 is a circuit diagram showing the structure of a switching circuit of the switching section (2) of an embodiment of the present invention;

Figure 22 is a sectional view of essential portions showing the sectional structures of the PMOS transistors (PM1 and PM21) and the NMOS transistors (NM2 and NM22) shown in Fig. 21;

Figure 23 is an illustration of the assembled liquid crystal display module of each of the above embodiments, in which a front view, front side view, right side view, left side view, and rear side view viewed from the display surface side of a liquid crystal display panel are shown;

Figure 24 is an illustration of the assembled liquid crystal display module of each of the above embodiments, viewed from the backside of a liquid crystal display panel;

Figures 25(a) and 25(b) are sectional views of the

assembled liquid crystal display in Fig. 23, taken along the lines I-I and II-II in Fig. 23;

Figures 26(a) and 26(b) are sectional views of the assembled liquid crystal display in Fig. 23, taken along the lines III-III and IV-IV in Fig. 23;

Figure 27 is an illustration showing the state in which a flexible printed circuit board (FPC1) and a flexible printed circuit board before bent are mounted around a liquid crystal display panel in the liquid crystal display module of each of the above embodiments;

Figure 28 is an enlarged view of the portion where a liquid crystal display panel and the flexible printed circuit boards (FPC1 and FPC2) are connected each other in Fig. 27;

Figure 29 is a graph showing the relation between the voltage applied to a liquid crystal layer and the transmittance; and

Figure 30 is an illustration showing the relation between the driving voltage applied to a pixel electrode and the driving voltage applied to a common electrode in the case of the dot inversion method.

Detailed Description of the Preferred Embodiments

An embodiment of the present invention is described below by referring to the accompanying drawings.

In all drawings for explaining embodiments of the present invention, components having the same function are provided with

the same symbol and their repetitive description is omitted.

Figure 1 is a block diagram showing a schematic structure of the TFT-type liquid crystal display module of an embodiment of the present invention.

In the case of the liquid crystal display module (LCM) of the embodiment of the present invention, a drain driver 130 is set to the upper side of a liquid crystal display panel (TFT-LCD) 10 and a gate driver 140 and an interface section 100 are arranged at the lateral of the liquid crystal display panel 10.

The interface section 100 is mounted on an interface board and the drain driver 130 and the gate driver 140 are also respectively mounted on their exclusive printed circuit board.

Figure 2 is an illustration showing an example of the equivalent circuit of the liquid crystal display panel 10 shown in Fig. 1. As shown in Fig. 2, the liquid crystal display panel 10 has a plurality of pixels formed like a matrix.

Each pixel is arranged in an intersectional region formed between two adjacent signal lines {drain signal lines (D) or gate signal lines (G)} and two adjacent signal lines {gate signal lines (G) or drain signal lines (D)}.

Each pixel has thin-film transistors (TFT1 and TFT2) and the source electrodes of the thin-film transistors (TFT1 and TFT2) of each pixel are connected to a pixel electrode (ITO1). Moreover, because a liquid crystal layer (LC) is formed between the pixel electrode (ITO1) and the common electrode (ITO2), a

liquid crystal capacitance is equivalently connected between the pixel electrode (ITO1) and the common electrode (ITO2).

Furthermore, an additional capacitance (CADD) is connected between the source electrodes of the thin-film transistors (TFT1 and TFT2) on one hand and the front-stage gate signal line (G) on the other.

Figure 3 is an illustration showing the equivalent circuit of another example of the liquid crystal display panel 10.

In the case of the example shown in Fig. 2, the additional capacitance (CADD) is formed between the gate signal lines (G) and the source electrodes at all stages. However, the equivalent circuit of the example shown in Fig. 3 is different in that a holding capacitance (CSTG) is formed between a common signal line (COM) and a source electrode.

The present invention can be applied to the above both systems. In the case of the former system, pulses of gate signal lines (G) at all stages enter the pixel electrode (ITO1) through the additional capacitance (CADD). In the case of the latter system, however, better display is realized because no pulse enters a pixel electrode.

Figures 2 and 3 show equivalent circuits of longitudinal electric-field liquid crystal display panels. Moreover, Figures 2 and 3 are circuit diagrams drawn correspondingly to actual geometric arrangement. Figure 4 shows the equivalent circuit of another example of the liquid crystal display panel 10.

Moreover, Fig. 4 shows the equivalent circuit of a lateral electric-field liquid crystal display panel.

Furthermore, in the case of the longitudinal electric-field liquid crystal display panel shown in Fig. 2 or 3, the common electrode (ITO2) is formed on a color filter board. In the case of the lateral electric-field liquid crystal display panel, however, a facing electrode (CT) is provided for a TFT board and a facing-electrode signal line (CL) for applying a driving voltage (VCOM) is provided for the facing electrode (CT).

Therefore, a liquid crystal capacitance (Cpix) is equivalently connected between a pixel electrode (PX) and the facing electrode (CT). Moreover, an accumulation capacitance (Cstg) is formed between the pixel electrode (PX) and the facing electrode (CT).

In Figs. 2, 3, and 4, symbol AR denotes a display region.

In the liquid crystal display panels 10 shown in Figs. 2 to 4, the drain electrode of the thin-film transistor (TFT) of each pixel is connected to each drain signal line (D) and each drain signal line (D) is connected to the drain driver 130 for applying a gradation voltage to the liquid crystal of each pixel in the column direction.

Moreover, the gate electrode of the thin-film transistor (TFT) of each pixel arranged in the row direction is connected to each gate signal line (G) and each gate signal line (G) is connected to the gate driver 140 for supplying a scan driving

voltage (positive bias voltage or negative bias voltage) to the gate electrode of the thin-film transistor (TFT) of each pixel in the row direction for one horizontal scanning period.

The interface section 100 shown in Fig. 1 is constituted with a display controller 110 and a power supply circuit 120.

The display controller 110 is constituted with one semiconductor integrated circuit (LSI) controls and drives the drain driver 130 and the gate driver 140 in accordance with a display control signal such as a clock signal, display timing signal, horizontal sync signal, or vertical sync signal transmitted from the computer body side and display data (R, G, B).

When the display controller 110 receives a display timing signal, it decides the signal as a display start position and outputs the received display data of simple one column to the drain driver 130 through a display-data bus line 133.

In this case, the display controller 110 a display-data latching clock (D2) serving as a display control signal for latching display data to the data latching circuit of the drain driver 130 through a signal line 131.

The display data sent from the body computer side is 8 bits and transferred in pixels, that is, every unit time by forming data values for red (R), green (G), and blue (B) into a set.

When the input of a display timing signal is completed or a predetermined time passes after the display timing signal is inputted, the display controller 110 decides that the display

data for one horizontal period is completed and outputs an output-timing control clock (D1) serving as a display control signal for outputting the display data stored in the latching circuit of the drain driver 130 to the drain signal line (D) of the liquid crystal display panel 10 to the drain driver 130 through a signal line 132.

Moreover, when the display controller 110 receives a first display timing signal after receiving a vertical sync signal, it decides the timing signal as a first display line and outputs a frame start designation signal to the gate driver 140 through a signal line 142.

Furthermore, the display controller 110 outputs a clock (G1) serving as a shift clock to the gate driver 140 through a signal line 141 every horizontal scanning period so as to successively apply a positive bias voltage to each gate signal line (G) of the liquid crystal display panel 10 every horizontal scanning period.

Thereby, a plurality of thin-film transistors (TFTs) connected to each gate signal line (G) of the liquid crystal display panel 10 are turned on for one horizontal scanning period.

According to the above operations, an image is displayed on the liquid crystal display panel 10.

The power supply circuit 120 shown in Fig. 1 is constituted with a positive-voltage generation circuit 121, a negative-

voltage generation circuit 122, a common electrode(facing electrode) voltage generation circuit 123, and a gate electrode voltage generation circuit 124.

The positive-voltage generation circuit 121 and negative-voltage generation circuit 122 are respectively constituted with a series-resistance voltage division circuit. The positive-voltage generation circuit 121 outputs five positive-polarity gradation reference voltages (V 0 to V 4) and the negative voltage generation circuit 122 outputs five negative-polarity gradation reference voltage (V 5 to V 9).

The positive-polarity gradation reference voltages (V 0 to V 4) and the negative-polarity gradation reference voltages (V 5 to V 9) are supplied to each drain driver 130.

Moreover, a conversion-to-AC signal (conversion-to-AC timing signal; M) is also supplied to each drain driver 130 from the display controller 110 through a signal line 135.

The common-electrode voltage generation circuit 123 generates a driving voltage to be applied to the common electrode (ITO2){or the facing electrode (CT)} and the gate-electrode voltage generation circuit 124 generates driving voltages (positive bias voltage and negative bias voltage) to be applied to the gate electrode of a thin-film transistor (TFT).

As described above, two methods such as the common symmetry method and the common inversion method are known as the driving method for applying an AC voltage to a liquid crystal layer. In

the case of the common symmetry method, the amplitude of a voltage to be applied to the pixel electrode (IT01/PX) is two times larger than the case of the common inversion method and therefore, there is a disadvantage that a low withstand voltage driver cannot be used. However, the dot inversion method or V-line inversion method can be used which is superior in small power consumption and display quality.

The liquid crystal display module of an embodiment of the present invention uses the dot inversion method as its driving method.

By using the dot inversion method, voltages to be applied to adjacent drain signal lines (D) have polarities opposite to each other. Therefore, it is possible to reduce power consumption because the current flowing through the common electrode (IT02) {or facing electrode (CT)} and the current flowing through the gate electrode of a thin-film transistor (TFT) are offset each other.

Moreover, because the current flowing through the common electrode (IT02) {or facing electrode (CT)} is small, thereby suppressing voltage drop. Therefore, the voltage level of the common electrode (IT02){or facing electrode (CT)} is stabilized and it is possible to minimize the deterioration of display quality.

Figure 5 is a block diagram showing a schematic structure of an example of the drain driver 130 shown in Fig. 1.

The drain driver 130 is constituted with one semiconductor integrated circuit (LSI).

In Fig. 5, a positive-polarity gradation voltage generation circuit 151a generates first positive-polarity gradation voltages of 33 gradations in accordance with five positive-polarity gradation reference voltages (V 0 to V 4) inputted from the positive-voltage generation circuit 121 and outputs the voltages to an output circuit 157 through a voltage bus line 158a. A negative-polarity gradation voltage generation circuit 151b generates first negative-polarity gradation voltages of 33 gradations in accordance with five negative-polarity gradation reference voltages (V 5 to V 9) inputted from the negative-voltage generation circuit 122
and outputs the voltages to the output circuit 157 through a voltage bus line 158b.

Moreover, a shift register circuit 153 in a control circuit 152 of the drain driver 130 generates a signal for fetching data from an input register circuit 154 in accordance with the display data latching clock (D2) received from the display controller 110 and outputs the signal to the input register circuit 154.

The input register circuit 154 latches the display data of 8 bits for each color by the value equivalent to the number of outputs synchronously with the display-data latching clock (D2) received from the display controller 110 in accordance with the data-capturing signal output from the shift register circuit 153.

A storage register circuit 155 latches the display data in the input register circuit 154 correspondingly to the output-timing control clock (D1) received from the display controller 110.

The display data fetched by the storage register circuit 155 is inputted to the outputted circuit 157 through a level shift circuit 156.

The output circuit 157 generates one gradation voltage (one of 256 gradation voltages) corresponding to display data in accordance with the first positive-polarity gradation voltages of 33 gradations or first negative-polarity gradation voltages of 33 gradations and outputs the gradation voltage to each drain signal line (D).

Figure 6 is a block diagram for explaining the structure of the drain driver 130 shown in Fig. 5, centering around the structure of the output circuit 157.

In Fig. 6, symbol 153 denotes a shift register circuit in the control circuit 152 shown in Fig. 5 and 156 denotes a level shift circuit shown in Fig. 5. Moreover, a data latching circuit 265 shows the input register circuit 154 and storage register circuit 155 shown in Fig. 5. Furthermore, a decoder section (gradation voltage selection circuit) 261, an amplifier circuit pair 263, and a switching section (2) 264 for switching the outputs of the amplifier circuit pair 263 constitute the output circuit 157 shown in Fig. 5.

In this case, a switching section (1) 262 and the switching section (2) 264 are controlled in accordance with a conversion-to-AC signal (M).

Moreover, Y1, Y2, Y3, Y4, Y5, and Y6 show first, second, third, fourth, fifth, and sixth drain signal lines (D).

The drain driver 130 shown in Fig. 6 switches data-fetching signals inputted to the data latching section 265 (more minutely, the input register 154 shown in Fig. 5) by the switching section (1) 262 and inputs the display data for each color to the adjacent data-latching sections 265 for each color.

The decoder section 261 is constituted with a high-voltage decoder circuit 278 for generating positive-polarity gradation voltages corresponding to the display data output from each data latching section 265 (more minutely, the storage register 155 shown in Fig. 5) in accordance with the first positive-polarity gradation voltages of 33 gradations output from the gradation-voltage generation circuit 151a through the voltage bus line 158a and a low-voltage decoder circuit 279 for generating negative-polarity gradation voltages corresponding to the display data outputted from each data latching section 265 in accordance with the first negative-polarity gradation voltages of 33 gradations outputted from the gradation voltage generation circuit 151b through the voltage bus line 158b.

The high-voltage decoder circuit 278 and the low-voltage decoder circuit 279 are provided for each adjacent data latching

section 265.

The amplifier circuit pair 263 is constituted with a high-voltage amplifier circuit 271 and a low-voltage amplifier circuit 272. The high-voltage amplifier circuit 271 receives a positive-polarity gradation voltage generated by the high-voltage decoder circuit 278 and outputs a positive-polarity gradation voltage. The low-voltage amplifier circuit 272 receives a negative-polarity gradation voltage generated by the low-voltage decoder circuit 279 and outputs a negative-polarity gradation voltage.

In the case of the dot inversion method, gradation voltages for adjacent colors have polarities opposite to each other and the high-voltage amplifier circuit 271 and the low-voltage amplifier circuit 272 of the amplifier circuit pair 263 are arranged in the sequence of the high-voltage amplifier circuit 271, low-voltage amplifier circuit 272, high-voltage amplifier circuit 271, and low-voltage amplifier circuit 272. Therefore, it is possible to output a positive-polarity or negative-polarity gradation voltage by switching data-fetching signals inputted to the data latching section 165 by the with switching section (1) 262, inputting the display data for each color to adjacent data latching sections 265 for each color, thereby switching the voltages outputted from the high-voltage amplifier circuit 271 or low-voltage amplifier circuit 272 by the switching section (2) 264 and outputting the voltages to drain signal lines (D) such as the first drain signal line (Y1) and the fourth drain signal line

(Y4) from which gradation voltages for various colors are outputted.

Figure 7 is a circuit diagram showing the structure of a switching circuit of the switching section (2) 264 of the conventional example.

As shown in Fig. 7, the switching circuit of the switching section (2) 264 of the conventional example has a PMOS transistor (PM1) connected between the high-voltage amplifier circuit 271 and the n-th drain signal (Yn), a PMOS transistor (PM2) connected between the high-voltage amplifier circuit 271 and the (n+3)-th drain signal (Yn+1), an NMOS transistor (NM1) connected between the low-voltage amplifier circuit 272 and the (n+3)-th drain signal (Yn+3), and an NMOS transistor (NM2) connected between the low-voltage amplifier circuit 272 and the n-th drain signal (Yn).

The output of a NOR circuit (NOR1) inverted by an inverter (INV) is level-shifted by a level shift circuit (LS) and inputted to the gate electrode of the PMOS transistor (PM1) and the output of a NOR circuit (NOR2) inverted by the inverter (INV) is level-shifted by the level shift circuit (LS) and inputted to the gate electrode of the PMOS transistor (PM2).

Similarly, the output of the NAND circuit (NAND2) inverted by the inverter (INV) is level-shifted by the level shift circuit (LS) and inputted to the gate electrode of the NMOS transistor (MM1) and the output of the NAND circuit (NAND1) inverted by the inverter (INV) is level-shifted by the level shift circuit (LS)

and inputted to the gate electrode of the NMOS transistor (NM2).

Moreover, in Fig. 7, voltages to be applied to the MOS transistors (PM1, PM2, NM1, and NM2) are combined and illustrated.

In this case, a conversion-to-AC signal (M) is inputted to a NAND circuit (NAND1) and the NOR circuit (NOR1), and a conversion-to-AC signal (M) inverted by the inverter (INV) is inputted to a NAND circuit (NAND2) and the NOR circuit (NOR2).

Moreover, an output enable signal (ENB) is inputted to the NAND circuits (NAND1 and NAND2) and an output enable signal inverted by the inverter (INV) is inputted to the NOR circuits (NOR1 and NOR2).

Table 1 shows the truth tables of the NAND circuits (NAND1 and NAND2) and the NOR circuits (NOR1 and NOR2) and the following on/off states of the MOS transistors (PM1, PM2, NM1, and NM2).

[Table 1]

ENB	M	NOR1	PM1	NAND2	NM1	NAND1	PM2	NOR2	NM2
L	*	L	OFF	H	OFF	H	OFF	L	OFF
H	H	L	OFF	H	OFF	L	ON	H	ON
	L	H	ON	L	ON	H	OFF	L	OFF

Symbol * denotes that there is no relation with a conversion-to-AC signal (M).

As shown in Table 1, when an output enable signal (ENB) is Low-level (hereinafter referred to as L-level), the NAND circuits (NAND1 and NAND2) become High-level (hereinafter referred to as H-level), the NOR circuits (NOR1 and NOR2) become L-level, and

the MOS transistors (PM1, PM2, NM1, and NM2) are turned off.

When scanning lines are switched, the high voltage amplifier circuit 271 and the low-voltage amplifier circuit 272 are under an unstable state.

The output enable signal (ENB) is used to prevent the output of each of the amplifier circuits (271 and 272) from being outputted to each drain signal line (D) while scanning lines are switched.

Moreover, as shown in Table 1, when the output enable signal (ENB) is H-level, the NAND circuits (NAND1 and NAND2) become H-level or L-level and the NOR circuit (NOR1) becomes H-level or L-level correspondingly to the H-level or L-level of the conversion-to-AC signal (M).

As a result, the PMOS transistor (PM1) and NMOS transistor (NM1) are turned off or on, the PMOS transistor (PM2) and NMOS transistor (NM2) are turned on or off, and the output of the high-voltage amplifier circuit 271 is outputted to the drain signal line (Yn+3), and that of the low-voltage amplifier circuit 272 is outputted to the drain signal line (Yn), or the output of the high-voltage amplifier circuit 271 is outputted to the drain signal line (Yn), and that of the low-voltage amplifier circuit 272 is outputted to the drain signal line (Yn+3).

In the case of the conventional liquid crystal display module (LCM), the gradation voltage to be applied to the liquid crystal layer (LC) of each pixel ranges between 0 and 5 V at the

negative-polarity side and between 5 and 10 V at the positive-polarity side. Therefore, a negative-polarity gradation voltage of 0 to 5 V is outputted from the low-voltage amplifier circuit 272 and a positive-polarity gradation voltage of 5 to 10 V is outputted from the high-voltage amplifier circuit 271.

In this case, when the PMOS transistor (PM1) is turned off and the NMOS transistor (NM2) is turned on, a voltage of up to 10 V is applied between the source and the drain of the PMOS transistor (PM1).

Therefore, the MOS transistors (PM1, PM2, NM1, and NM2) respectively use a MOS transistor with high withstand voltage having a source-drain withstand voltage of 10 V.

Because the gap length between a pixel electrode (PX) and a facing electrode (CT) has been increased or the liquid crystal material of a liquid crystal layer (LC) has been improved in accordance with the improvement in the resolution of a lateral electric-field-type liquid crystal display panel, it is necessary to increase the range of a gradation voltage to be applied to the liquid crystal layer (LC) of each pixel to 5 to 2.5 V at the negative-polarity side and 2.5 to 10 V at the positive-polarity side.

When applying the gradation voltages having the range of 5 to 2.5 V at the negative-polarity side and the range of 2.5 to 10 V at the positive-polarity side to the liquid crystal layer (LC) of each pixel, a voltage of up to 15 V is applied to MOS

transistors to be turned off in the switching circuit shown in Fig. 7. Therefore, it is necessary to use a MOS transistor with high withstand voltage having a source-drain withstand voltage of 15 V for the MOS transistors (PM1, PM2, NM1, and NM2) constituting the switching circuit.

The MOS transistor with high withstand voltage having a source-drain withstand voltage of 15 V has a large fluctuation of threshold (VT) or conductance (gm). Moreover, it is necessary to replace every MOS transistor with high withstand voltage in the drain driver 130 with the MOS transistor with high withstand voltage having a source-drain withstand voltage of 15 V due to the restriction on the fabrication process. Therefore, a problem occurs that the chip size of a semiconductor integrated circuit constituting the drain driver 130 increases and thus, it is impossible to deal with frame minimization.

Figure 8 is a circuit diagram showing the structure of a switching circuit of the switching section (2) 264 of an embodiment of the present invention.

In the case of an embodiment of the present invention, a gradation voltage having a range of 2.5 to 10 V is outputted from the high-voltage amplifier circuit 271 and a gradation voltage having a range of 5 to 2.5 V is outputted from the low-voltage amplifier circuit 272. Therefore, voltage-dropping MOS transistors (PM21, PM22, NM21, and NM22) are connected in series with the MOS transistors (PM1, PM2, NM1, and NM2) constituting a

switching circuit.

A constant bias voltage of 0 V is applied to the gate electrodes of the voltage-dropping PMOS transistors (PM21 and PM22) and a constant bias voltage of 5 V is applied to the voltage-dropping NMOS transistors (NM21 and NM22). Other structures are the same as those in Fig. 7.

An embodiment of the present invention uses the inverted signal of an output timing control clock (D1) as the output enable signal (ENB). However, it is also possible to generate the output enable signal (ENB) inside of the embodiment by counting display-data latching clocks (D2).

When the PMOS transistor (MP1) is turned off and the NMOS transistor (NM2) is turned on, a voltage of up to 15 V is applied to the both ends of a pair of transistor constituted with the PMOS transistors (PM1) and (PM21).

However, because the PMOS transistor (PM1) is turned off and no current flows through the pair of transistor, the source voltage (VS) of the PMOS transistor (PM21) is shown by the following expression (1).

[Numerical Formula 1]

$$VGS \quad VT = 0$$

$$VG \quad VS \quad VT = 0$$

$$VS = VG \quad VT \qquad \ldots(1)$$

In the above expression, VGS denotes the gate-source voltage of the PMOS transistor (PM21), VG denotes the gate

voltage of the PMOS transistor (PM21), and VT denotes the threshold voltage of the PMOS transistor (PM21).

That is, the source voltage (VS) of the PMOS transistor (PM21) becomes equal to the voltage obtained by subtracting the threshold voltage (VT) of the transistor (PM21) from the gate voltage (VG) of the transistor (PM21) and the source voltage of the PMOS transistor (PM21) becomes almost equal to its gate voltage (VG)(= 0 V).

Because the source voltage (VS) of the PMOS transistor (PM21) is equal to the drain voltage (VD) of the PMOS transistor (PM1), it is possible to use the PMOS transistor with high withstand voltage having a source-drain withstand voltage of 10 V same as that of the conventional example as the PMOS transistor (PM1).

Moreover, when the PMOS transistor (PM1) is turned on and the NMOS transistor (NM2) is turned off, the source voltage (VS) of the NMOS transistor (NM22) becomes almost equal to its gate voltage (VG)(= 5V).

Therefore, it is possible to use the PMOS transistor with high withstand voltage having a source-drain withstand voltage of 10 V as the NMOS transistor (NM2) similarly to the case of the conventional example.

Moreover, because the bias voltage of 0 V to be applied to the gate electrode of the PMOS transistor (PM21) is a bias voltage for turning on the PMOS transistor (PM21), the output of

the high-voltage amplifier circuit 271 is output to the drain signal line (Yn) through the PMOS transistor (PM21) when the PMOS transistor (PM1) is turned on.

Figure 9 is a sectional view of essential portions showing the sectional structures of the PMOS transistors (PM1 and PM21) and the NMOS transistors (NM2 and NM22).

As shown in Fig. 9, a first n-well region 21a is formed on a p-type semiconductor substrate 20 and a p-well region 22 is formed in the first n-well region 21a.

In this case, a voltage of 5 V is applied to the p-type semiconductor substrate 20 and a voltage of 5 V is applied to the first n-well region 21a.

The NMOS transistors (NM2) and (NM22) are constituted with semiconductor regions (24a, 24b, and 24c) formed in the p-well region 22 and gate electrodes (26a and 26b).

In this case, the n-type semiconductor region (24b) is used as the drain region of the NMOS transistor (NM2) and the source region of the NMOS transistor (NM22). Moreover, a negative-polarity gradation voltage is applied to the p-well region 22 from the low-voltage amplifier circuit 272 by a p-type semiconductor region 25d.

Similarly, a second n-well region 21b is formed on the p-type semiconductor substrate 20 and a third n-well region 23 is formed in the second n-well region 21b. In this case, a positive-polarity gradation voltage is applied to the second n-

well region 21b and third n-well region 23 from the high-voltage amplifier circuit 271 by an n type semiconductor region 24d.

The PMOS transistors (PM1 and PM12) are constituted with p-type semiconductor regions (25a, 25b, and 25c) and gate electrodes (27a and 27b).

In this case, the p-type semiconductor region (25b) is used as the drain region of the PMOS transistor (PM1) and the source region of the PMOS transistor (PM21).

Moreover, Fig. 9 illustrates the maximum withstand voltages between the n-type semiconductor regions (24a, 24b, and 24c), between the p-type semiconductor regions (25a, 25b, and 25c), and between each of the n-type semiconductor regions (24a, 24b, and 24c), each of the p-type semiconductor regions (25a, 25b, and 25c), and each well region.

Figures 10 and 11 are sectional views of essential portions for explaining the outline of the fabrication steps of the PMOS transistors (PM1 and PM21) and the NMOS transistors (NM2 and NM22).

Then, a method for forming the PMOS transistors (PM1 and PM21) and the NMOS transistors (NM2 and NM22) are briefly described below by referring to Figs. 10 and 11.

First, the p-type semiconductor substrate 20 made of single crystal silicon is prepared to form the first n-well region 21a, second n-well region 21b, and p-well region 22, and third n-well region 23 through selective ion implantation of p- and n-type

region decision impurities. {Fig. 10(a)}

In this case, the first n-well region 21a, second n well region 21b, and third n-well region 23 use phosphorus (P) as an n-type region decision impurity. A quantity of impurity to be introduced into the first n-well region 21a and the second n-well region 21b is set to approx. 5.4×10^{12}[atoms/cm^2] and a quantity of impurity to be introduced into the third n-well region 23 is set to approx. 1.0×10^{12}[atoms/cm^2].

Moreover, the p-well region 22 uses boron fluoride (BF_2) and a quantity of impurity to be introduced into the region 22 is set to approx. 1.1×10^{13}[atoms/cm^2].

Then, a field insulating film 30 made of a silicon oxide film is formed on the principal plane of the element separation region of the p-type semiconductor substrate 20 by the publicly-known selective oxidation method. {Fig. 10(b)}

Then, thermal oxidation treatment is performed to form a gate-electrode insulating film 31 made of a silicon oxide film on the principal planes of the p-type well region 22 and the third n-well region 23 and then deposit a polysilicon film 32 on the gate-electrode insulating film 31 by, for example, the CVD method. {Fig. 10(c) and Fig. 10(d)}

Then, patterning is applied to the polysilicon film 32 to form gate electrodes (26a, 26b, 27a, and 27b) on the gate-electrode insulating films 31 of the p-well region 22 and the third n-well region 23. {Fig. 10(e)}

Then, a mask 33 is formed on the p-type semiconductor substrate 20. The mask 33 is formed with, for example, a photoresist film locally having an aperture on the third n-well region 23 and p-well region 22 to cover the remaining region of the p-well region 22. The photoresist film is coated by the spin coating method and baked and thereafter, formed by being exposed and developed.

Then, the p-type semiconductor regions (25a, 25b, 25c, and 25d) are formed by using the mask 33 and gate electrodes (27a and 27b) as impurity introduction masks, thereby introducing a p-type region decision impurity in accordance with the ion implantation method, and performing annealing. In this case, the impurity uses boron fluoride (BF_2) and ion implantation is performed twice to first form a p-type semiconductor region having an impurity introduction quantity of approx. 3.0×10^{14}[atoms/cm^2] and then, forming a p-type semiconductor region having an impurity introduction quantity of approx. 2.0×10^{15}[atoms/cm^2].

That is, the p-type semiconductor regions (25a, 25b, 25c, and 25d) are formed so that a p-type semiconductor region having a high impurity concentration is enclosed by a p-type semiconductor region having a low impurity concentration. Thereby, the impurity concentration gradient is moderated and the withstand voltage to a well region is improved. {Fig. 11(a)}

Then, the mask 33 is removed and then, a mask 34 is formed on the p-type semiconductor substrate 20. The mask 34 is made

of, for example, a photoresist film locally having an aperture on the p-well region 22 and third n-well region 23 and covering the remaining region of the third n-well region 23.

Then, the n-type semiconductor regions (24a, 24b, 24c, and 24d) are formed by using the mask 34 and the gate electrodes (26a and 26b) as impurity introduction masks, thereby introducing an n-type region decision impurity in accordance with the ion implantation method and performing annealing. In this case, ion implantation is performed twice similarly to the case of the above process to first form an n-type semiconductor region having an impurity introduction quantity of approx. 3.0×10^{13}[atoms/cm^2] by using phosphorus as an impurity and then form an n-type semiconductor region having an impurity introduction quantity of approx. 3.0×10^{15}[atoms/cm^2] by using arsenic (As) as an impurity.

That is, the n-type semiconductor regions (24a, 24b, 24c, and 24d) are formed so that an n-type semiconductor region having a high impurity concentration is enclosed by an n-type semiconductor region having a low impurity concentration. Thereby, the impurity concentration gradient is moderated and the withstand voltage to a well region is improved. {Fig. 11(b)}

Then, as shown in Fig. 11(c), the mask 34 is removed and thereafter, a layer insulating film 35 made of a silicon oxide film is formed on the p-type semiconductor substrate 20 and a connection hole 36 where the surfaces of the n-type semiconductor regions (24a, 24c, and 24d) and those of the p-type semiconductor

regions (25a, 25c, and 25d) are exposed is formed on the layer insulating film 35. {Fig. 11(d)}

Then, aluminum is vacuum-deposited on the p-type semiconductor substrate 20 and thereafter, aluminum other than wiring is removed through etching. {Fig. 11(e)}

As described above, according to an embodiment of the present invention, it is possible to use a MOS transistor having a source-drain withstand voltage of 10 V as the switching element of the switching section (2) 264 to whose both ends a voltage of 10 to 20 V is applied. Thus, it is possible to decrease the area of the switching section (2) 264 compared to the case of using a MOS transistor with high withstand voltage having a source-drain withstand voltage of 20 V as the switching element of the switching section (2) 264. Thereby, it is possible to decrease the chip size of the drain driver 130 and accordingly, reduce the cost of the liquid crystal display module (LCM).

Then, the high-voltage decoder circuit 278 of an embodiment of the present invention is described below by referring to Fig. 12.

Figure 12 is a circuit diagram showing the structure of an example of the high-voltage decoder circuit 278 of an embodiment of the present invention.

Figure 12 also shows a schematic structure of the positive-polarity gradation voltage generation circuit 151a.

As shown in Fig. 12, the positive-polarity gradation

voltage generation circuit 151a generates first positive-polarity gradation voltages of 33 gradations in accordance with five positive-polarity gradation reference voltages (V 0 to V 4) supplied from the positive-voltage generation circuit 121.

In this case, the relation between the voltage applied to a liquid crystal layer and the transmittance of the voltage is not linear. As shown in Fig. 29, the transmittance of the voltage applied to the liquid crystal layer does not greatly change at a portion where the transmittance is high or low, but the transmittance greatly changes at a portion where the transmittance is intermediate.

Therefore, the five positive-polarity gradation reference voltages (V 0 to V 4) are set so that the difference between the voltages decreases nearby intermediate gradation voltages (V 2 to V 3) but increases nearby gradation voltages (V 1 to V 2 and V 3 to V 4) other than the voltages (V 2 to V 3). Moreover, each voltage-division resistance of a resistance voltage-division circuit constituting the positive-polarity gradation voltage generation circuit 151a is provided with a predetermined weight in accordance with the relation between the voltage applied to the liquid crystal layer and the transmittance of the voltage.

In the case of the positive-polarity gradation voltage generation circuit in Fig. 12, five positive-polarity gradation reference voltages (V 0 to V 4) are divided into 8 levels to generate first gradation voltages of 33 gradations. However, it

is needless to say that the voltage division ratio between the five positive polarity gradation reference voltages (V 0 to V 4) can be properly changed in accordance with the relation between the voltage applied to the liquid crystal layer and the transmittance of the voltage.

The high-voltage decoder circuit 278 has a decoder circuit 301 for selecting first adjacent gradation voltages (VOUTA and VOUTB) of the first gradation voltages of 33 gradations, a multiplexer 302 for outputting the first gradation voltage (VOUTA) selected by the decoder circuit 301 to a terminal (P1) or terminal (P2) and outputting the first gradation voltage (VOUTB) selected by the decoder circuit 301 to the terminal (P2) or (P1), and a second gradation voltage generation circuit 303 for dividing the potential difference (ΔV) between the adjacent first gradation voltages (VOUTA and VOUTB) outputted from the multiplexer 302 and generating 1/8 ΔV, 2/8 ΔV, 3/8 ΔV, 4/8 ΔV (1/2 ΔV), 5/8 ΔV, 6/8 ΔV, 7/8 ΔV, and 8/8 (= 1)ΔV of the potential difference (ΔV).

The decoder circuit 301 is constituted with a first decoder circuit 311 for selecting first gradation voltages corresponding to high-order five bits (D3 to D7) of 8-bit display data and a second decoder circuit 312 for selecting first gradation voltages corresponding to high-order four bits (D4 to D7) of the 8-bit display data.

The first decoder circuit 311 is constituted so as to

select the 1st first-gradation voltage (V1) and the 33rd first gradation voltage (V33) once and select 3rd first-gradation voltage (V3) to 31st first-gradation voltage (V33) twice consecutively in accordance with high-order five bits (D3 to D7) of the 8-bit display data.

However, the second decoder circuit 312 is constituted so as to select 2nd first-gradation voltage (V2) to 32nd first-gradation voltage (V32) once in accordance with high-order four bits (D4 to D7) of the 8-bit display data.

In Fig. 12, symbol O denotes a switching element (e.g. PMOS transistor) to be turned on when a data bit is Low-level.

In this case, because the relation of V 0<V 1<V 2<V 3<V 4 is effectuated, when the value of the bit 4 (D3) of the display data is L-level, a gradation voltage having a potential lower than that of the gradation voltage VOUTB is outputted as the gradation voltage VOUTA. Moreover, when the value of the bit 4 (D3) of the display data is H-level, a gradation voltage having a potential higher than that of the gradation voltage VOUTB is outputted as the gradation voltage VOUTA.

Therefore, the multiplexer 302 is switched in accordance with H-level and L-level of the value of the bit 4 (D3) of the display data, the gradation voltage VOUTA is outputted to the terminal (P1) and the gradation voltage VOUTB is outputted to the terminal (P2) when the value of the bit 4 (D3) of the display data is L-level, and the gradation voltage VOUTB is outputted to

the terminal (P1) and the gradation voltage VOUTA is outputted to the terminal (P2) when the value of the bit 4 (D3) of the display data is H-level.

Thereby, whenever the gradation voltage of the terminal (P1) is set to (Va) and that of the terminal (P2) is set to (Vb), it is possible to effectuate the relation of Va<Vb. Thus, the design of the second gradation voltage generation circuit 303 is simplified.

Figure 13 is a circuit diagram showing an example of the structure of the second gradation voltage generation circuit 303 shown in Fig. 2.

The second gradation voltage generation circuit 303 has a capacitor (Co1) connected between the terminal (P2) and the input terminal of the amplifier circuit (high-voltage amplifier circuit 271), a capacitor (Co2) whose one end is connected to the input terminal of the amplifier circuit and whose other end is connected to the terminal (P1) through a switching element (S01) and moreover connected to the terminal (P2) through a switching element (S02), a capacitor (Co3) whose one end is connected to the input terminal of the amplifier circuit and whose other end is connected to the terminal (P1) through a switching element (S11) and moreover connected to the terminal (P2) through a switching element (S12), a capacitor (Co4) whose one end is connected to the input terminal of the amplifier circuit and whose other end is connected to the terminal (P1) through a

switching element (S21) and moreover connected to the terminal (P2) through a switching element (S22), and a switching element (SS1) connected between the terminal (P2) and the input terminal of an amplifier.

In this case, the capacitor (Co1) has the same capacitance as that of the capacitor (Co2), the capacitor (Co3) has a capacitance two times larger than that of the capacitor (Co1), and the capacitor (Co4) has a capacitance four times larger than that of the capacitor (Co1).

Moreover, as shown in Fig. 13, the switching element (SS1) is controlled in accordance with a reset pulse (/CR) and the switching elements (S01, S02, S11, S12, S21, and S22) are controlled in accordance with the reset pulse (/CR), a timing pulse (/TCK), and a switching control circuits (SG1 to SG3) to which low-order three bits (D0 to D2) of display data are inputted.

The switching control circuits (SG1 to SG3) are respectively provided with a NAND circuit (NAND), AND circuit (AND), and NOR circuit (NOR). Table 2 shows the truth tables of the NAND circuit (NAND), AND circuit (AND), and NOR circuit (NOR).

[Table 2]

/CR	/TCK	/D	NAND	AND	NOR	Sn1	Sn2
L	H	*	H	L	L	OFF	ON
H	H	*	H	L	H	OFF	OFF
	L	H	L	L	H	ON	OFF

		L	H	H	L	OFF	ON

Symbol * denotes that there is no relation with display data.

Operations of the second gradation voltage generation circuit 303 are briefly described below by referring to Table 2. First, when the reset pulse (/CR) is L-level, the switching element (SS1) is turned on. Moreover, because the H-level reset pulse (/CR) is inputted to the NOR circuit (NOR), the output of the NOR circuit (NOR) becomes L-level and the switching elements (S02, S12, and S22) are turned on.

In this case, the timing pulse (/TCK) is H-level and the L-level timing pulse (/TCK) is inputted to the NAND circuit (NAND), the output of the NAND circuit (NAND) becomes H-level and the switching elements (S01, S11, and S21) are turned off. Thereby, because the both ends of the capacitors (Co1 to Co4) are connected to the terminal (P2), the capacitors (Co1 to Co4) are discharged and the potential difference between the capacitors is set to 0 V.

Then, when the reset pulse (/CR) is H-level and the timing pulse (/TCK) becomes L-level, the switching elements (S01, S02, S11, S12, S21, and S22) are turned on or off in accordance with the value of each of low-order three bits (D0 to D2) of display data.

Thereby, when assuming the gradation voltage of the terminal (P1) as (Va), the gradation voltage of the terminal (P2)

as (Vb), and the potential difference between Va and Vb as ΔV, gradation voltages of Va+1/8 ΔV, Va-2/8 ΔV,..., Vb(Va+8/8 ΔV) are outputted from the second gradation voltage generation circuit 302.

To display 256 gradations by using the high-voltage decoder circuit 278 of the full-code system, 16 transistors are necessary every 256 gradations. Therefore, the total number of MOS transistors per drain signal line (D) becomes 4,096 (256×16).

Therefore, problems occur that the area occupied by the decoder section 261 increases and the chip size of a semiconductor integrated circuit (IC chip) increases.

In the case of the high-voltage decoder circuit 278 of an embodiment of the present invention, the number of switching elements constituting a decoder circuit becomes 160 {=(17+15)×5} for the first decoder circuit 311 and 64 (= 4×16) for the second decoder circuit 312. Therefore, the total number of switching elements (MOS transistors) constituting a decoder circuit per drain signal line (D) becomes 224. Thus, it is possible to greatly decrease the number of MOS transistors per drain signal line (D) compared to 4,096 MOS transistors per drain signal line (D) required for the conventional example.

Moreover, by decreasing the number of switching elements, it is possible to reduce the internal current of the drain driver 130. Therefore, it is possible to reduce the total power consumption of the liquid crystal display module (LCM), thereby

improving the reliability of the liquid crystal display module (LCM).

Moreover, the low-voltage decoder circuit 279 can be constituted similarly to the high-voltage decoder circuit 278. In this case, the negative-polarity gradation voltage generation circuit 151b generates first negative-polarity gradation voltages of 33 gradations in accordance with five negative-polarity gradation reference voltages (V 5 to V 9) inputted from the negative voltage generation circuit 122.

In this case, each voltage-division resistance of a resistance voltage-division circuit constituting the negative-polarity gradation voltage generation circuit 151b is provided with a predetermined weight in accordance with the relation between the voltage applied to a liquid crystal layer and the transmittance of the voltage.

In the case of the low-voltage decoder circuit 279, because the relation of V 5>V 6>V 7>V 8>V 9 is effectuated, an inequality of Va>Vb is always obtained when assuming the gradation voltage of the terminal (P1) as (Va) and that of the terminal (P2) as (Vb).

Figure 14 is a circuit diagram showing the circuit structure of another example of the high-voltage decoder circuit 278 of an embodiment of the present invention and Figure 15 is a schematic view for explaining the gate width of a MOS transistor constituting the high-voltage decoder circuit 278 shown in Fig.

14.

In Fig. 12, symbol O denotes a PMOS transistor and symbol ● denotes an NMOS transistor.

In the case of the high-voltage decoder circuit 278 shown in Fig. 12, the number of MOS transistors in which the same voltage is applied to their gate electrodes every decoding row increases for higher bits of display data.

Therefore, even if the same voltage is applied to a gate electrode every column and MOS transistors continued every decoding row are replaced with one MOS transistor, there is no functional problem.

An embodiment of the present invention is constituted by replacing MOS transistors in which the same voltage is applied to their gate electrodes every column and continued every decoding row with one MOS transistor.

Moreover, in the case of an embodiment of the present invention, when assuming the gate width of a minimum-size MOS transistor as W, the gate width of a MOS transistor at a higher-order column than the minimum-size MOS transistor is set to 2W and the gate width of a MOS transistor at a higher-order column than the above MOS transistor is set to 4W as shown in Fig. 15. That is, the gate width (W) of a MOS transistor (MOS transistor at the higher-order bit side) in which a high-order bit of display data is applied to its gate electrode is set to a value $2^{(m-j)}$ times larger than the gate width of the minimum size MOS

transistor.

In this case, symbol m denotes the number of bits of display data and j denotes the bit number of the most significant bit among the bits constituted with the minimum size MOS transistor.

In the case of an embodiment of the present invention, when assuming the resistance of a minimum size MOS transistor as R, the combined resistance of MOS transistors at each decoding row become approx. 2R ($\fallingdotseq$ R+R/2+R/4+R/8+R/16) for the decoder circuit 312 and approx. 2R ($\fallingdotseq$ R+R/2+R/4+R/8) for the decoder circuit 312.

Moreover, Fig. 12 shows the resistance of the MOS transistor at each column when assuming the resistance of the minimum size MOS transistor as R.

In this case, in the case of the high-voltage decoder circuit 278 shown in Fig. 12, when assuming the resistance of the minimum size MOS transistor as R, the combined resistance of MOS transistors at each decoding row becomes 5R (=R+R+R+R+R) for the decoder circuit 311 and 4R (=R+R+R+R) for the decoder circuit 312.

Therefore, in the case of the high-voltage decoder circuit 278 shown in Fig. 14, it is possible to reduce the combined resistance of MOS transistors at each decoding row and flow a large discharge current when redistributing electric charges to the capacitors constituting the second gradation voltage

generation circuit 303. Thus, it is possible to accelerate the operation speed of a decoder circuit and equalize the combined resistance of the decoder circuit 311 with that of the decoder circuit 312, thereby reducing the speed difference between two gradations to be generated.

Moreover, in the case of a MOS transistor, a threshold voltage (V_T) changes in the positive direction due to a substrate-source voltage (V_{BS}), thereby decreasing a drain current (I_{DS}) in general. That is, the on-resistance of the MOS transistor increases.

Therefore, in the case of the high-voltage decoder circuit 278 shown in Fig. 14, a PMOS transistor region and an NMOS transistor region are separated from each other at the both sides of the gradation voltage at which the substrate-source voltage (V_{BS}) is equalized {gradation voltage of V16 (or V18) or V15 (or V17) in Fig. 14} as shown in Fig. 14.

Thereby, the high-voltage decoder circuit 278 shown in Fig. 14 makes it possible to prevent the resistance of a MOS transistor constituting a decoder circuit from increasing due to the substrate bias effect.

Figure 16 is a circuit diagram showing the structure of an example of the low-voltage decoder circuit 279 of an embodiment of the present invention.

As shown in Fig. 16, the low-voltage decoder circuit 279 can be constituted similarly to the high-voltage decoder circuit

278 shown in Fig. 16.

However, voltages have the relation of V1>V2>V3...>V32>33.

In the case of the low-voltage decoder circuit 279, a PMOS transistor region and an NMOS transistor region are opposite to the case of the high-voltage decoder circuit 278 when separating the PMOS transistor region from the NMOS transistor region at the both sides of the gradation voltage at which the substrate-source voltage (V_{BS}) is equalized {V16 (or V18) or V15 (or V17) in Fig. 16}.

Moreover, in the decode circuits shown in Figs. 12 to 16, each MOS transistor constituting the decoder circuit 301 is constituted with MOS transistor with a high withstand voltage or a MOS transistor only whose gate electrode has a structure with high withstand voltage.

Furthermore, a MOS transistor at the low-bit side of the decoder circuit 301 can use a MOS transistor having a low drain-source withstand voltage. In this case, it is possible to further decrease the size of the decoder circuit 301.

Furthermore, the second gradation voltage generation circuit 303 can use a resistance instead of a capacitor. In this case, however, it is necessary to use a resistance having a high resistance value and moreover, set resistances so that the sequence of magnitudes of the resistances is reverse to that of magnitudes of the capacitors.

For example, when using resistances for the second

gradation voltage generation circuit 303 instead of capacitors, it is necessary that resistances to be replaced with the capacitors (Co1) and (Co2) have a resistance value four times larger than that of the value of a resistance to be replaced with the capacitor (Co4) and a resistance to be replaced with the capacitor (Co3) has a value two times larger than that of a resistance to be replaced with the capacitor (Co4).

Figure 17 is a circuit diagram showing the structure of a switching circuit of the switching section (2) 264 of an embodiment of the present invention.

An embodiment of the present invention is different from the foregoing embodiments of the present invention in that a constant bias voltage is applied to a p-well region 22 and a third n-well region 23 on which MOS transistors (PM1, PM2, NM1, and NM2) and voltage-dropping MOS transistors (PM21, PM22, NM21, and NM22) are formed. However, other structures are the same as those of the foregoing embodiments of the present invention.

Figure 18 is a sectional view of essential portions showing sectional structures of the PMOS transistors (PM1 and PM21) and NMOS transistors (NM2 and NM22) shown in Fig. 17.

As shown in Fig. 18, a first n-well region 21 is formed on a p-type semiconductor substrate 20, and a p-well region 22 and third n-well region 23 are formed in the first n-well region 21. In this case, a voltage of 5 V is applied to the p-type semiconductor substrate 20 and p-well region 22 and a voltage of

10 V is applied to a first n-well region 21a and the third n-well region 23.

Moreover, Fig. 18 illustrates maximum withstand voltages between n-type semiconductor regions (24a, 24b, and 24c), between p-type semiconductor regions (25a, 25b, and 25c), and the n type semiconductor regions (24a, 24b, and 24c), p type semiconductor regions (25a, 25b, and 25c), and well regions.

In the case of the switching circuit of each foregoing embodiment of the present invention, the p-well region 22 has a potential equal to that of the source region (24a in Fig. 18) of the NMOS transistors (NM1 and NM2) and the output voltage of an low-voltage amplifier circuit 272 is applied to the p-well region 22.

Moreover, the third n-well region 23 has a potential equal to that of the source region (25a in Fig. 18) of the PMOS transistors (PM1 and PM2) and the output voltage of a high-voltage amplifier circuit 271 is applied to the third n-well region 23.

Therefore, the switching circuit of each foregoing embodiment of the present invention has a disadvantage that the latch-up phenomenon easily occurs if the output voltage {gradation voltage to be supplied to a drain signal (D)} of the switching circuit is fluctuated due to noises or the like. However, an embodiment of the present invention makes it possible to prevent the latch-up phenomenon from easily occurring because

a constant voltage is applied to the p-well region 22 and third n-well region 23.

Figure 19 is a circuit diagram showing the structure of a switching circuit of the switching section (2) 264 of an embodiment of the present invention.

An embodiment of the present invention is different from the foregoing embodiments of the present invention in that NMOS transistors (NM31 and NM32) are connected to PMOS transistors (PM1 and PM2) and PMOS transistors (PM31 and PM32) are connected to NMOS transistors (NM1 and NM2) in parallel.

A voltage obtained by inverting the voltage to be applied to the gate electrodes of the PMOS transistors (PM1 and PM2) is applied to the gate electrodes of the NMOS transistors (NM31 and NM32) and the NMOS transistors (NM31 and NM32) are turned on/off synchronously with the PMOS transistors (PM1 and PM2).

Similarly, a voltage obtained by inverting the voltage to be applied to the gate electrodes of the NMOS transistors (NM1 and NM2) is applied to the gate electrodes of the PMOS transistors (PM31 and PM32), and the PMOS transistors (PM31 and PM32) are turned on/off synchronously with the NMOS transistors (NM1 and NM2).

Figure 20 is a sectional view of essential portions of the PMOS transistors (PM1, PM21, and PM32) and the NMOS transistors (NM2, NM22, and NM31) shown in Fig. 19.

As shown in Fig. 20, a first n-well region 21a is formed on

a p-type semiconductor substrate 20 and a first p-well region 22a and a fourth n-well region 23b are formed in the first n-well region 21a. In this case, a voltage of 5 V is applied to the p-type semiconductor substrate 20 and the first p-well region 22a and a voltage of 5 V is applied to the first n-well region 21a and the fourth n-well region 23b.

A PMOS transistor (PM32) is constituted with p-type semiconductor regions (25e, 25f, and 24c) and a gate electrode (26c) formed in the fourth n well region 23b.

Similarly, a second n-well region 21b is formed on the p-type semiconductor substrate 20 and a third n-well region 23a and a second p-well region 22b are formed in the second n-well region 21b. In this case, a voltage of 10 V is applied to the second n-well region 21b and third n-well region 23a and a voltage of 0 V is applied to the second p-well region 22b.

An NMOS transistor (NM31) is constituted with n-type semiconductor regions (24e and 24f) and a gate electrode (27c) formed in the second p-well region 22b.

Moreover, Fig. 20 illustrates the maximum withstand voltages between the n-type semiconductor regions (24a, 24b, 24c, 24e, and 24f), between the p-type semiconductor regions (25a, 25b, 25c, 25e, and 25f), and between the n-type semiconductor regions (24a, 24b, 24c, 24e, and 24f), p-type semiconductor regions (25a, 25b, 25c, 25e, and 25f), and well regions.

The switching circuit of each foregoing embodiment of the

present invention makes it possible to prevent the latch up phenomenon from easily occurring because a constant voltage is applied to the p-well region 22 and the third n-well region 23.

In the case of a MOS transistor, however, a threshold voltage (V_T) changes in the positive direction due to a substrate source voltage (V_{BS}) (so-called substrate bias effect), thereby decreasing a drain current (I_{DS}), that is, increasing the on-resistance of the MOS transistor.

Moreover, each foregoing embodiment of the present invention has a disadvantage that the on-resistance of a MOS transistor increases due to the substrate bias effect because the source voltages and the well voltages of the PMOS transistors (PM1 and PM2) and the NMOS transistors (NM1 and NM2) do not have the same potential.

However, an embodiment of the present invention makes it possible to prevent the on-resistance of a MOS transistor from increasing in accordance with the substrate bias effect because the PMOS transistors (PM1 and PM2) connect in parallel with the NMOS transistors (NM31 and NM32) and the NMOS transistors (NM1 and NM2) connect in parallel with the PMOS transistors (PM31 and PM32).

Figure 21 is a circuit diagram showing the structure of a switching circuit of the switching section (2) 264 of an embodiment of the present invention.

The embodiment of the present invention is different from

the foregoing embodiments of the present invention in that the gate voltages of the voltage-dropping MOS transistors (PM21, PM22, NM21, and NM22) connected to the MOS transistors (PM1, PM2, NM1, and NM2) in series are switched in two levels in accordance with the values of the gradation voltages outputted from the high-voltage amplifier circuit 271 and the low-voltage amplifier circuit 272.

Figure 22 is a sectional view of essential portions showing sectional structures of the PMOS transistors (PM1, PM2, and PM32) and the NMOS transistors (NM2, NM22, and NM31) shown in Fig. 21, which is the same as Fig. 20 except that voltages applied to the gate electrodes of the PMOS transistor (PM21) and NMOS transistor (NM22) can be changed.

Tables 3 and 4 show the truth tables of the NAND circuits (NAND3 and NAND4) and the NOR circuits (NOR3 and NOR4), on/off states of the MOS transistors (PM1 PM2, NM1, and NM2), and voltage values applied to the gate electrodes of the MOS transistors (PM21 and NM22).

[Table 3]

M	PM1 (NM31)	PM2 (NM31)	NM1 (NM31)	NM2 (NM31)
H	OFF	ON	OFF	ON
L	ON	OFF	ON	OFF

[Table 4]

M	D7 (Yn)	D7 (Yn+1)	NAND3	NOR3	NAND4	NOR4	PM21	PM22	NM21	NM22

M	H	H	H	L	H	L	0V	0V	5V	5V
	L	L	H	H	L	L	0V	-5V	5V	10V
L	H	H	H	L	H	L	0V	0V	5V	5V
	L	L	L	L	H	H	-5V	0V	10V	5V

Moreover, in Fig. 21, inverters (HINV1 and HINV2) respectively constituted with a MOS transistor with high withstand voltage output level-shifted output signals. That is, the inverters (HINV1 and HINV2) also serve as level shift circuits.

As shown in Table 3, when a conversion-to-AC signal (M) is H-level, the PMOS transistor (PM2) and NMOS transistor (NM2) are turned on.

Moreover, as shown in Table 4, a voltage of 0 V is applied to the gate electrode of the PMOS transistor (PM22) connected in series to the turned-on PMOS transistor (PM2) when the value of the most significant bit (D7) of the display data corresponding to the drain signal line (Yn+3) is H-level and a voltage of 5 V is applied to the turned-on PMOS transistor (PM2) when the value of the most significant bit (D7) of the display data corresponding to the drain signal line (Yn+3) is L-level.

Furthermore, as shown in Table 3, when the conversion-to-AC signal (M) is L-level, the PMOS transistor (PM2) is turned off. In this case, however, a voltage of 0 V is applied to the gate electrode of the PMOS transistor (PM22) independently of the value of the most significant bit (D7) of display data as shown

in Table 4.

Similarly, a voltage of 5 V is applied to the gate electrode of the NMOS transistor (NM22) connected in series to the turned on NMOS transistor (NM2) when the value of the most significant bit (D7) of the display data corresponding to the drain signal line (Yn) is H-level, and a voltage of 10 V is applied to the gate electrode of the NMOS transistor (NM22) when the value of the most significant bit (D7) of the display data corresponding to the drain signal line (Yn) is L-level.

Moreover, as shown in Table 3, when the conversion-to-AC signal (M) is L-level, the NMOS transistor (NM2) is turned off. In this case, however, a voltage of 5 V is applied to the gate electrode of the NMOS transistor (NM22) independently of the value of the most significant bit (D7) of the display data as shown in Table 4.

Thus, in the case of an embodiment of the present invention, when a voltage (Vlin) outputted from the high-voltage amplifier circuit 271 meets the expression $|Vlin-Vlg| \leq |Vlmax-Vlmin|/2$ (where, Vlmax denotes the maximum voltage outputted from the high-voltage amplifier circuit 271, Vlmin denotes the minimum voltage outputted from the high-voltage amplifier circuit 271, and Vlg denotes a bias voltage of 0 V), a voltage of 5 V is applied to the gate electrodes of the voltage-dropping PMOS transistors (PM21 and PM22) connected in series to the turned-on PMOS transistors (PM1 and PM2). Moreover, when the voltage

(V1in) outputted from the high voltage amplifier circuit 271 meets the expression $|V1in\ V1g| \leq |V1max - V1min|/2$, a bias voltage of 0 V is applied to the gate electrodes of the voltage-dropping PMOS transistor (PM21 and PM22) connected in series to the turned-on PMOS transistors (PM1 and PM2).

Similarly, when a voltage (V2in) outputted from the low-voltage amplifier circuit 272 meets the expression $|V2in - V2g| \leq |V2max\ V2min|/2$ (where, V2max denotes the maximum voltage outputted from the low-voltage amplifier circuit 272, V2min denotes the minimum voltage outputted from the low-voltage amplifier circuit 272, and V2g denotes a bias voltage of 5 V), a bias voltage of 10 V is applied to the gate electrodes of the voltage-dropping NMOS transistors (NM21 and NM2) connected in series to the turned-on NMOS transistors (NM1 and NM2). Moreover, when the voltage (V2in) outputted from the low-voltage amplifier circuit 272 meets the expression $|V2in - V2g| > |V2max - V2min|/2$, a bias voltage of 5 V is applied to the gate electrodes of the voltage-dropping NMOS transistors (NM21 and NM22) connected in series to the turned-on NMOS transistors (NM1 and NM2).

In general, as a gate-source voltage (VGS) lowers, a drain current (I_{DS}) decreases. Therefore, the on-resistance of a MOS transistor increases.

In the case of an embodiment of the present invention, however, when gradation voltages outputted from the amplifier circuits

(271 and 272) are voltages close to 0 V ($|V1in-V1g| \leq |V1max-V1min|/2$ and $|V2in-V2g| \leq |V2max\ V2min|/2$), the gate source voltages (VGS) of the voltage dropping MOS transistors (PM21, PM22, NM21, and NM22) connected in series to the turned-on MOS transistors (PM1, PM2, NM1, and NM2) are set so as to rise. Therefore, when gradation voltages outputted from the amplifier circuits (271 and 272) are voltage close to 0 V, it is possible to prevent the on-resistance of a MOS transistor from increasing.

Moreover, in the case of an embodiment of the present invention, it is possible to set the gate-source voltages (VGS) of the voltage-dropping MOS transistors (PM21, PM22, NM21, and NM22) connected in series to the turned-on MOS transistors (PM1, PM2, NM1, and NM2) so as to rise independently of the values of the gradation voltages outputted from the amplifier circuits (271 and 272).

Furthermore, in the case of an embodiment of the present invention, it is possible to prevent the outputs of the amplifier circuits (271 and 272) from being outputted to drain signal lines (D) by an output enable signal (ENB) while scanning lines are switched similarly to the case of each foregoing embodiment of the present invention.

Furthermore, there are some foregoing embodiments of the present invention whose switching circuit fabrication method is not described, it is needless to say that the switching circuits of the foregoing embodiments can be fabricated by the above-

described method.

Figure 23 is an illustration of the assembled liquid crystal display module of each foregoing embodiment of the present invention, showing a front view, front side view, right side view, left side view, and rear side view of the module viewed from the display side of a liquid crystal display panel. Figure 24 is an illustration of the assembled liquid crystal display module of each foregoing embodiment of the present invention, viewed from the back side of a liquid crystal display panel.

The liquid crystal display module of each foregoing embodiment of the present invention is provided with a mold case (ML) and a shield case (SHD). HLD1, HLD2, HLD3, and HLD4 denote holes formed on the mold case (ML) and shield case (SHD). The liquid crystal display module is mounted on a notebook-type personal computer by passing a screw through these four mounting holes.

An inverter circuit unit for driving a backlight is set to the recess between the mounting holes (HLD1 and HLD2) to supply a driving voltage to a cold-cathode fluorescent lamp (LP) through a linkage connector (LCT) and lamp cables (LCP1 and LCP2).

Display data, display control signal, and power are supplied to an interface section 100 from the computer body side through an interface connector (CT1).

Figure 25(a) is a sectional view of the liquid crystal display module in Fig. 23, taken along the line I-I in Fig. 23 and Figure 25(b) is a sectional view of the liquid crystal display module in Fig. 23, taken along the line II II in Fig. 23. Figure 26(a) is a sectional view of the liquid crystal display module in Fig. 23, taken along the line III-III in Fig. 23, and Figure 26(b) is a sectional view of the liquid crystal display module in Fig. 23, taken along the line IV-IV in Fig. 23.

In Figs. 25 and 26, symbol SHD denotes a shield case (upper case) for covering the circumference and the driving circuit of a liquid crystal display panel. Symbol ML denotes a mold case (lower case) for storing a backlight unit. Symbols LF1 and LF2 denote first and second lower shield cases for covering a lower case (ML).

Symbol WSPC denotes a frame spacer for covering the circumference of the backlight unit. Symbols SUB1 and SUB2 denote glass substrates constituting the liquid crystal display panel.

In Fig. 26, when a longitudinal electric-field-type liquid crystal display panel 10 is used, the glass substrate (SUB1) is a substrate on which a thin-film transistor (TFT) and a pixel electrode (ITO1) are formed and the glass substrate (SUB2) is a substrate on which a color filter and a common electrode (ITO2) are formed. When a lateral electric-field-type liquid crystal display panel 10 is used, the glass substrate (SUB1) is a

substrate on which a thin-film transistor (TFT), a pixel electrode (ITO1), and a facing electrode (CT) are formed and the glass substrate (SUB2) is a substrate on which a color filter is formed.

Symbol FUS denotes a sealing material, BM denotes an opaque film formed on the glass substrate (SUB2), POL1 denotes an upper polarizing plate attached to the glass substrate (SUB2), POL2 denotes a lower polarizing plate attached to the glass substrate (SUB1), VINC1 denotes a visual-field expansion film, and VINC2 denotes a visual-field expansion film attached to the glass substrate (SUB2). The lateral electric-field-type liquid crystal display panel 10 does not always require the visual-field expansion film.

Each foregoing embodiment of the present invention eliminates the visual-field dependency which is a problem peculiar to a liquid crystal display panel in which the contrast changes depending on the angle at which a user see by attaching the visual-field expansion films (VINC1 and VINC2) to the glass substrates (SUB1 and SUB2).

It is possible to attach the visual-field expansion films (VINC1 and VINC2) to the outside of the polarizing plates (POL1 and POL2). However, by setting the visual-field expansion films (VINC1 and VINC2) between the polarizing plates (POL1 and POL2) and the glass substrates (SUB1 and SUB2), it is possible to improve the visual-field expansion effect.

Symbol LP denotes a cold-cathode fluorescent lamp, LS denotes a lamp reflection sheet, GLB denotes a light guiding plate, RFS denotes a reflecting sheet, and SPS denotes a prism sheet. Symbol POR denotes a polarized-light reflecting plate that is used to improve the brightness of the liquid crystal display panel.

The polarized light reflecting plate (POR) has a function for passing only the light of a specific polarization axis and reflecting the light of other polarization axes. Therefore, by adjusting the polarization axis the polarized-light reflecting plate (POR) passes to the polarization axis of the lower polarizing plate (POL2), the light having been absorbed so far by the lower polarizing plate (POL2) is changed to the polarized light passing through the lower polarizing plate (POL2) while the light reciprocates between the polarized-light reflecting plate (POR) and the light guiding plate (GLB) and emitted from the polarized-light reflecting plate (POR). Therefore, it is possible to improve the contrast of the liquid crystal display panel.

The frame spacer (WSPC) firmly secures the light guiding plate (GLB) to the mold case (ML) by holding the circumferential portion of the light guiding plate (GLB) and inserting a hook into the holed of the mold case (ML) to prevent the light guiding plate (GLB) from colliding with the liquid crystal display panel.

Moreover, because a diffusing sheet (SPS), a prism sheet

(PRS), and the polarized-light reflecting plate (POR) are held by the frame spacer (WSPC), it is possible to mount the backlight on the liquid crystal display module without distorting the diffusion sheet(SPS), the prism sheet (PRS), or polarized light reflecting plate (POR).

Symbol GC1 denotes a rubber cushion set between the frame spacer (WSPC), and the glass substrate (SUB1). Symbol LPC3 denotes a lamp cable for supplying a driving voltage to the cold cathode fluorescent lamp (LP), which is made of a flat cable to minimize the mounting space and set between the frame spacer (WSPC) and the lamp reflecting sheet (LS).

The lamp cable (LPC3) is attached to the lamp-reflecting sheet (LS) by a both-sided adhesive tape. Therefore, when replacing the cold-cathode fluorescent lamp (LP), it is possible to replace the cable (LPC3) together with the lamp-reflecting sheet (LS). Thus, it is unnecessary to remove the lamp cable (LPC3) from the lamp-reflecting sheet (LS), thereby replacing the cold-cathode fluorescent lamp (LP).

Symbol OL denotes an O ring which serves as a cushion between the cold-cathode fluorescent lamp (LP) and the lamp-reflecting sheet (LS). The O ring (OL) is made of transparent synthetic resin so that the luminous brightness of the cold-cathode fluorescent lamp (LP) is not deteriorated.

Moreover, the O ring is made of an insulating material having a low permittivity in order to prevent a high-frequency

current from leaking from the cold-cathode fluorescent lamp (LP). Furthermore, the O ring (OL) serves as a cushion for preventing the cold cathode fluorescent lamp (LP) from colliding with the light guiding plate (GLB).

Symbol IC1 denotes a semiconductor chip constituting the drain driver 130 for supplying a picture signal voltage to the drain signal line (D) of the liquid crystal display panel 10, which is mounted on the glass substrate (SUB1).

Because the semiconductor chip (IC1) is mounted on only one side of the glass substrate (SUB1), it is possible to downsize the frame region of the side facing the side on which the semiconductor chip (IC1) is mounted.

Moreover, because the cold-cathode fluorescent lamp (LP) and the lamp reflecting sheet (LS) are arranged below the portion on which the semiconductor chip (IC1) of the glass substrate (SUB1) is mounted so as to be superimposed each other, it is possible to compactly store the cold-cathode fluorescent lamp (LP) and the lamp reflecting sheet (LS) in the liquid crystal display module.

Symbol IC2 denotes a semiconductor ship constituting the gate driver 140 for supplying a scan driving voltage to the gate signal line (G) of the liquid crystal display panel 10, which is mounted on the glass substrate (SUB1).

Because the semiconductor chip (IC2) is also mounted on only one side of the glass substrate (SUB1), it is possible to

downsize the frame region of the side facing the side on which the semiconductor chip (IC2) is mounted.

Symbol FPC1 denotes a flexible printed circuit board at the gate signal line side, which is connected to the external terminal of the glass substrate (SUB1) by an anisotropic conductive film to supply power and a driving signal to the semiconductor chip (IC2).

Symbol FPC2 denotes a flexible printed circuit board at the drain signal line side, which is connected to the external terminal of the glass substrate (SUB1) by an anisotropic conductive film to supply power and a driving signal to the semiconductor chip (IC1).

Chip parts (EP) such as a resistance and a capacitor are mounted on the flexible printed circuit boards (FPC1 and FPC2).

To downsize the frame region of the liquid crystal display panel 10, the flexible printed circuit board (FPC2) is bent so as to wrap the lamp reflecting sheet (LS), and a part (portion b) of the flexible printed circuit board (FPC2) is secured between the mold case (ML) and the second shield case at the back of the backlight unit.

Therefore, a cutout for securing the spacer of a chip part (EP) to be mounted on the flexible printed circuit board (FPC2) is formed on the mold case (ML).

The flexible printed circuit board (FPC2) is constituted with a thin portion (portion a) to be easily bent and a thick

portion (portion b) for multilayer wiring.

Moreover, in the case of each foregoing embodiment of the present invention, a lower shield case is constituted with a first lower shield case (LF1) and a second lower shield case (LF2) so as to cover the back of the liquid crystal display module with these two lower shield cases (LF1 and LF2). Therefore, the lamp reflecting sheet (LS) can be exposed by removing the second lower shield case (LF2). Thus, the cold cathode fluorescent lamp (LP) can be easily replaced.

Symbol PCB denotes an interface board on which the display controller 110 and the power supply circuit 120 are mounted. The interface board (PCB) is also constituted with a multilayer printed circuit board.

In the case of each foregoing embodiment of the present invention, the interface board (PCB) is set under the flexible printed circuit board (FPC1) and bonded to the glass substrate (SUB1) by a both-sided adhesive tape (BAT) in order to downsize the frame region of the liquid crystal display panel 10.

The interface board (PCB) is provided with a connector (CTR3) and a connector (CTR4), and the connector (CTR4) is electrically connected with the connector (CT4) of the flexible printed circuit board (FPC2).

Similarly, the connector (CTR3) is electrically connected with the connector (CT3) of the flexible printed circuit board (FPC1).

Figure 27 is an illustration showing a state in which the flexible printed circuit board (FPC1) and the flexible printed circuit board (FPC2) before bent are mounted around the liquid crystal display panel 10.

Figure 28 is an illustration showing the enlarged portion where the liquid crystal display panel 10 is connected with the flexible printed circuit boards (FPC1 and FPC2) in Fig. 27.

In Figs. 27 and 28, symbol TCON denotes a semiconductor chip constituting the display controller 110, DTM denotes a drain terminal, and GTM denotes a gate terminal.

In Figs. 25 and 26, symbol SUB denotes a reinforcing plate that is set between the lower shield case (LF1) and the connector (CT4) to prevent the connector (CT4) from being removed from the connector (CTR4). Symbol SPC4 denotes a spacer set between the shield case (SHD) and the upper polarizing plate (POL1), which is made of nonwoven fabric and attached to the shield case (SHD) by an adhesive.

In the case of each foregoing embodiment of the present invention, the upper polarizing plate (POL1) and the visual-field expansion film (VINC1) are extended from the glass substrate (SUB2) and held by the shield case (SHD).

Each foregoing embodiment of the present invention can secure a large-enough strength by the above structure even if a frame region is downsized.

Symbol DSPC denotes a drain spacer that is set between the

shield case (SHD) and the glass substrate (SUB1) to prevent the shield case (SHD) from colliding with the glass substrate (SUB1).

Moreover, because the drain spacer (DSPC) is set so as to cover the semiconductor chip (IC1), a cutout (NOT) is formed on the semiconductor chip (IC1).

Thereby, the shield case (SHD) or drain spacer (DSPC) does not collide with the semiconductor chip (IC1).

Furthermore, because the drain spacer (DSPC) holds the flexible printed circuit board (FPC2) on the external terminal of the glass substrate (SUB1), it prevents the flexible printed circuit board (FPC2) from being removed from the glass substrate (SUB1). Symbol FUS denotes a sealing material for sealing the liquid crystal enclosing port of the liquid crystal display panel.

The inventions made by the present inventor are specifically described above in accordance with the foregoing embodiments of the present invention. However, the present invention is not restricted to the foregoing embodiments of the present invention. It is a matter of course that various modification of the present invention are allowed as long as they are not deviated from the gist of the present invention.

Advantages obtained from typical ones of the inventions disclosed in this application are briefly described below.

(1) According to the present invention, a semiconductor integrated circuit makes it possible to use a transistor with low

withstand voltage as the switching element of a switching circuit in which a voltage equal to or higher than the source drain withstand voltage of the transistor with low withstand voltage is applied between the input and output terminals, and decrease the chip size of a semiconductor chip on which the switching circuit is mounted compared to the case of using a transistor with high withstand voltage having a source drain withstand voltage equal to or higher than that of the transistor with low withstand voltage.

(2) According to the present invention, a liquid crystal display makes it possible to use a transistor with low withstand voltage as the switching element of a switching section in which a voltage equal to or higher than the source drain withstand voltage of the transistor with low withstand voltage is applied between the input and output terminals, thereby outputting a positive-polarity picture signal voltage and a negative polarity picture signal voltage to a pair of picture signal lines and decreasing the area of the switching section in picture-signal line driving means compared to the case of using a transistor with high withstand voltage having a source-drain withstand voltage equal to or higher than that of the transistor with low withstand voltage as the switching element of the switching section.

(3) According to the present invention, a liquid crystal display makes it possible to decrease the chip size of picture

signal driving means, thereby reducing the cost of the liquid crystal display and improving the reliability of the liquid crystal display.

What is claimed is:

1. A liquid crystal display device comprising:

a liquid crystal display panel; and

a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel; said picture signal line driving circuit having a switching circuit in which a first transistor to whose gate electrode a control voltage is applied and a second transistor to whose gate electrode a bias voltage is applied are connected in series.

2. The liquid crystal display device according to claim 1, wherein a first bias voltage is applied to the gate electrode of the second transistor and a second bias voltage is applied to a well layer provided with the first and the second transistors.

3. The liquid crystal display device according to claim 1, wherein the first and the second transistors are first conducting-type transistors, and a second conducting-type transistor is connected to the first transistor in parallel.

4. The liquid crystal display device according to claim 1, wherein the potential of the input terminal of the first transistor is equal to the potential applied to the well layer provided with the first and the second

transistors.

5. A liquid crystal display device, comprising a liquid crystal display panel and a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel; said picture signal line driving circuit further including

a first input terminal, a second input terminal, and a common output terminal,

a first switching element connected between the first input terminal and the common output terminal, and

a second switching element connected between the second input terminal and the common output terminal,

the first and second switching elements including a transistor at input port to whose gate electrode a control voltage is applied connected in series with a transistor at output port to whose gate electrode a bias voltage is applied.

6. The liquid crystal display device according to claim 5, wherein the bias voltage applied to the gate electrode of the transistor at the input port is different from the bias voltage applied to a well layer provided with the transistor at the input port and the transistor at the output port.

7. The liquid crystal display device according to

claim 5, wherein the transistor at the input port and the transistor at the output port of the first switching element are first conducting-type transistors, the transistor at the input port and the transistor at the output port of the second switching element are second conducting type transistors, and the second conducting type transistor is connected to the transistor at the input port of the first switching element in parallel and the first conducting-type transistor is connected to the transistor at the input port of the second switching element in parallel.

8. The liquid crystal display device according to claim 5, wherein the potential of the input terminal of the transistor at the input port applied to the well layer provided with the transistor at the output port.

9. A liquid crystal display device, comprising a liquid crystal display panel and a picture signal line driving circuit for supplying a picture signal voltage to the liquid crystal display panel; the picture signal line driving circuit further comprising

a first output circuit for outputting a positive-polarity picture signal voltage,

a second output circuit for outputting a negative-polarity picture signal voltage, and

a switching circuit for switching the positive-polarity picture signal voltage supplied from the first output circuit and the negative-polarity picture signal voltage supplied from the second output circuit to a pair of picture signal lines and outputting the voltages, the switching circuit further including

a first switching element connected between the first output circuit and the first picture signal line of the picture signal line pair,

a third switching element connected between the first output circuit and the second picture signal line of the picture signal line pair,

a second switching element connected between the second output circuit and the second picture signal line, and

a fourth switching element connected between the second output circuit and the first picture signal line,

wherein a positive-polarity picture signal voltage supplied from the first output circuit is output to the first or second picture signal line by selectively turning on/off the first, second, third, and fourth switching elements,

a negative-polarity picture signal voltage supplied from the second output circuit is output to the second

or first picture signal line by selectively turning on/off the first, second, third, and fourth switching elements,

and the switching elements are constituted by connecting a transistor at output circuit side to whose gate electrode a control voltage is applied in series with a transistor at picture signal line side to whose gate electrode a constant bias voltage is applied.

10. The liquid crystal display device according to claim 9, wherein the bias voltage applied to the gate electrode of the transistor at the picture signal side is different from the bias voltage applied to a well layer provided with a transistor at output port and a transistor at picture signal side.

11. The liquid crystal display device according to claim 9, wherein the transistors at the output side and the picture signal side of the first and third switching elements are first conducting-type transistors and the transistors at the output port and the picture signal side of the second and fourth switching elements are second conducting-type transistors, and the second conducting-type transistors are connected in parallel with the transistors at the output port of the first and third switching elements and the first conducting-type

transistors are connected in parallel with the transistors at the output port of the second and fourth switching elements.

12. The liquid crystal display device according to claim 9, wherein the potential of the input terminal of the transistor at the output circuit side is equal to the potential applied to the well layer provided with the transistor at the picture signal line side.

Abstract of the Disclosure

To provide a The liquid crystal display device having a semiconductor integrated circuit capable of outputting a voltage equal to or higher than the source-drain withstand voltage of a component transistor.

A switching circuit having first conducting type first and second transistors connected in series between a first input terminal and a common output terminal and second conducting type third and fourth transistors connected between a second input terminal and the common output terminal and a switching control circuit for controlling the switching circuit are provided. The switching control circuit applies first and second bias voltages for turning on the second and fourth transistors to the gate electrodes of the second and fourth transistors, and applies a control voltage for selectively turning on/off the first or third transistor to the gate electrodes of the first and third transistors.

FIG. 1

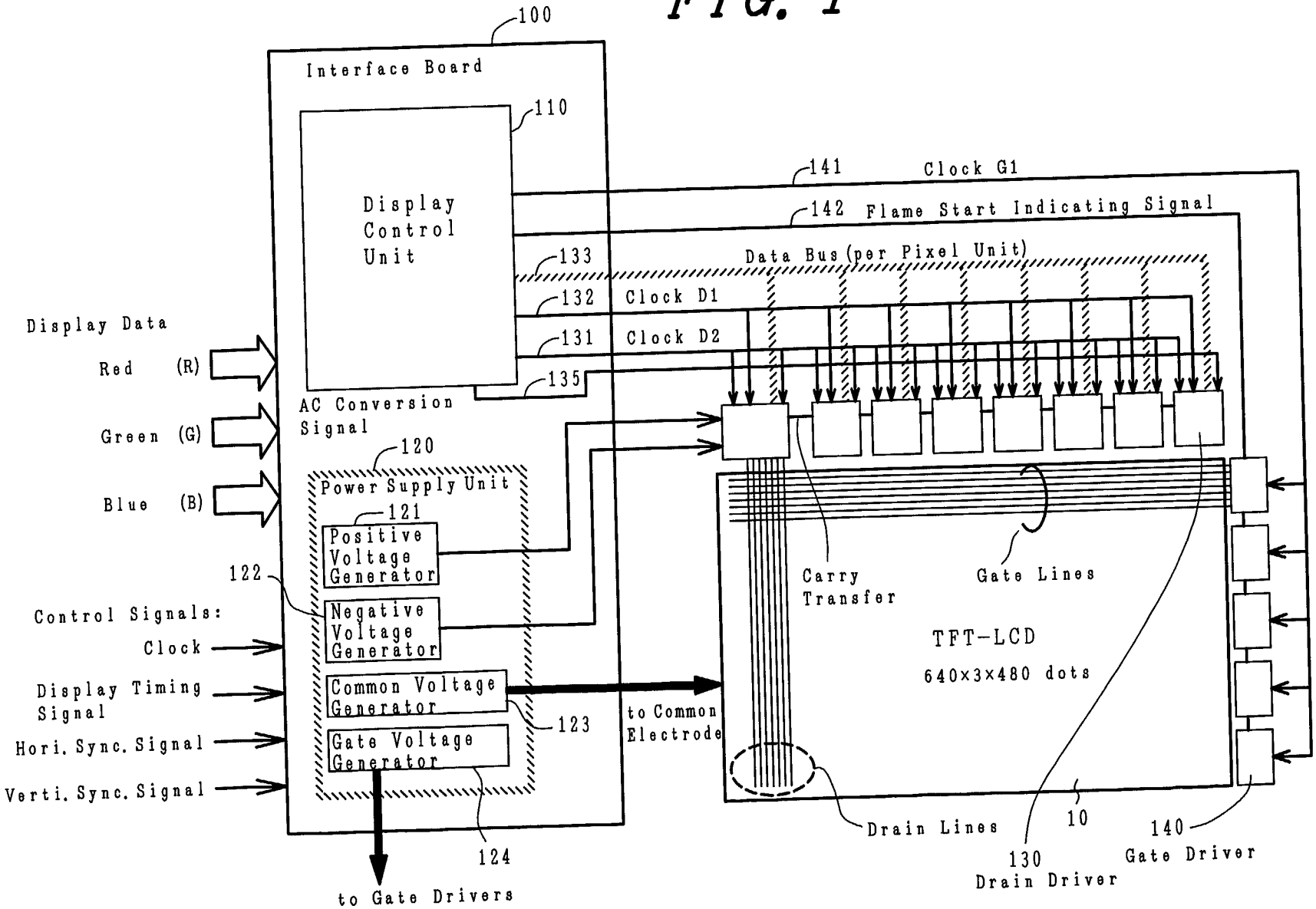


FIG. 2

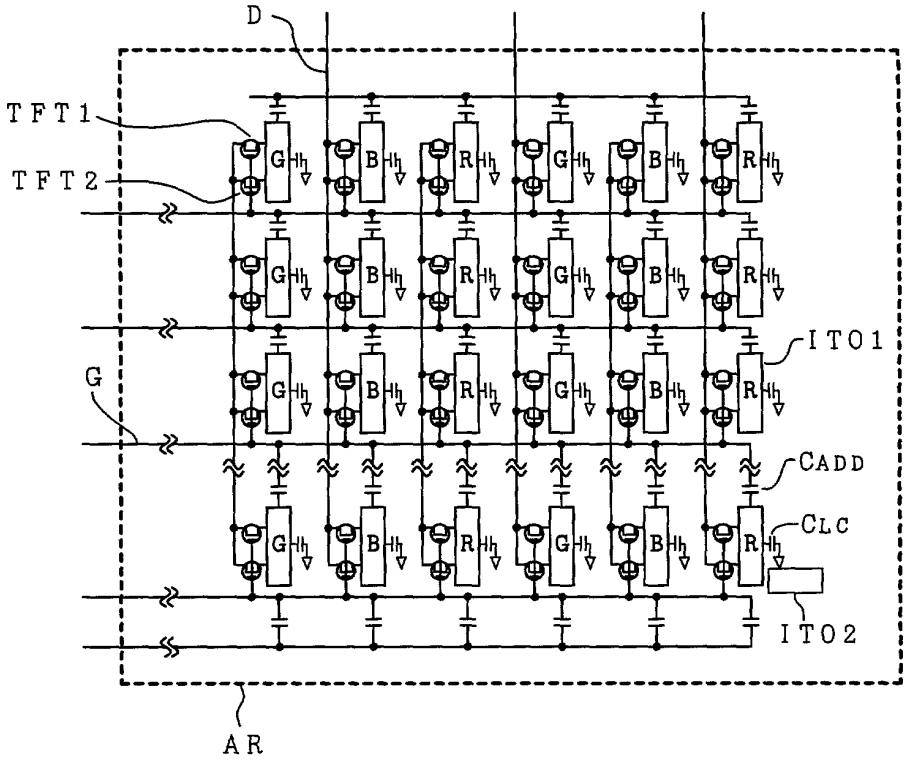


FIG. 3

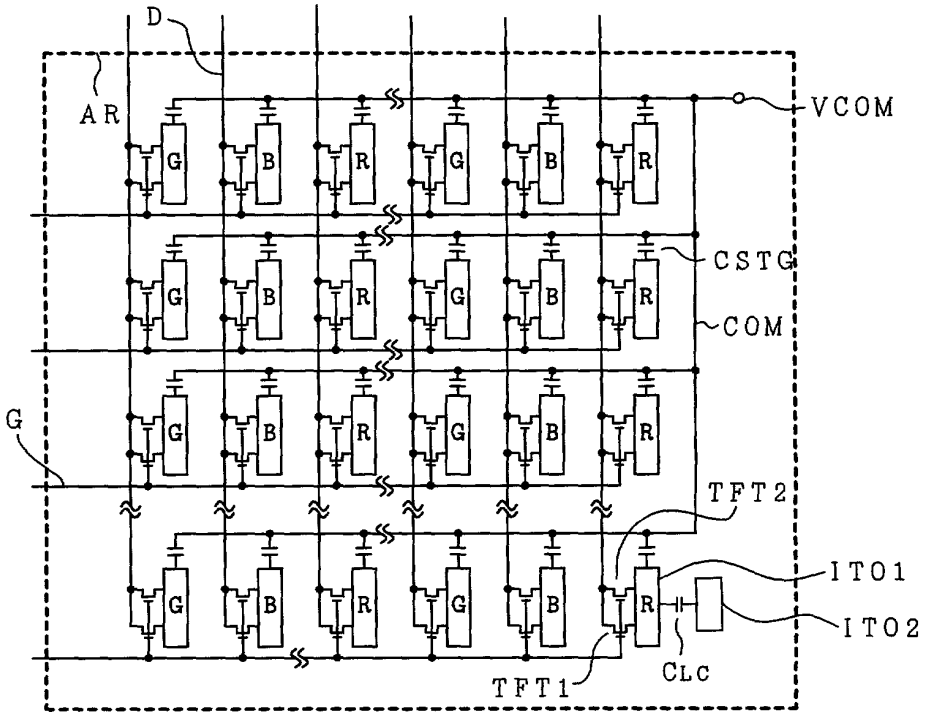


FIG. 4

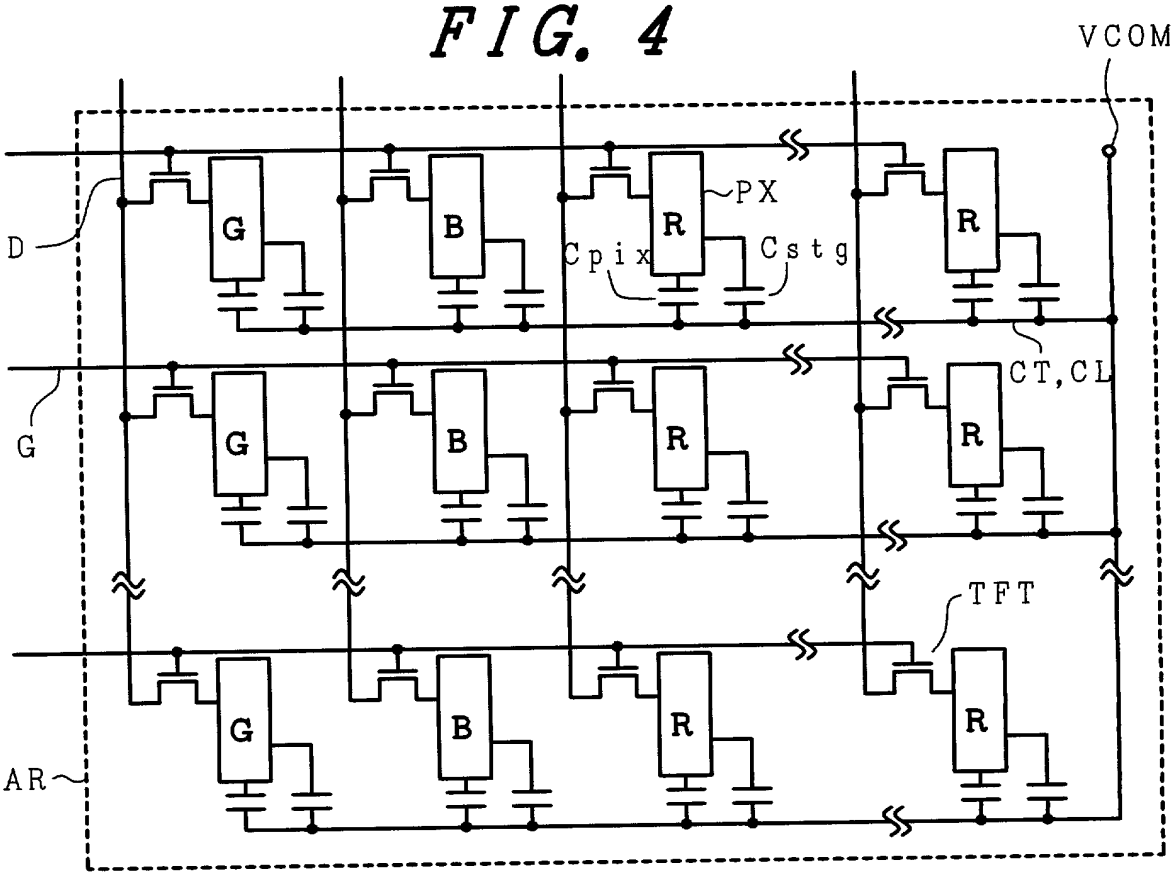

VCOM
D
G
AR
PX
Cpix
Cstg
CT,CL
TFT
G
B
R

FIG. 5

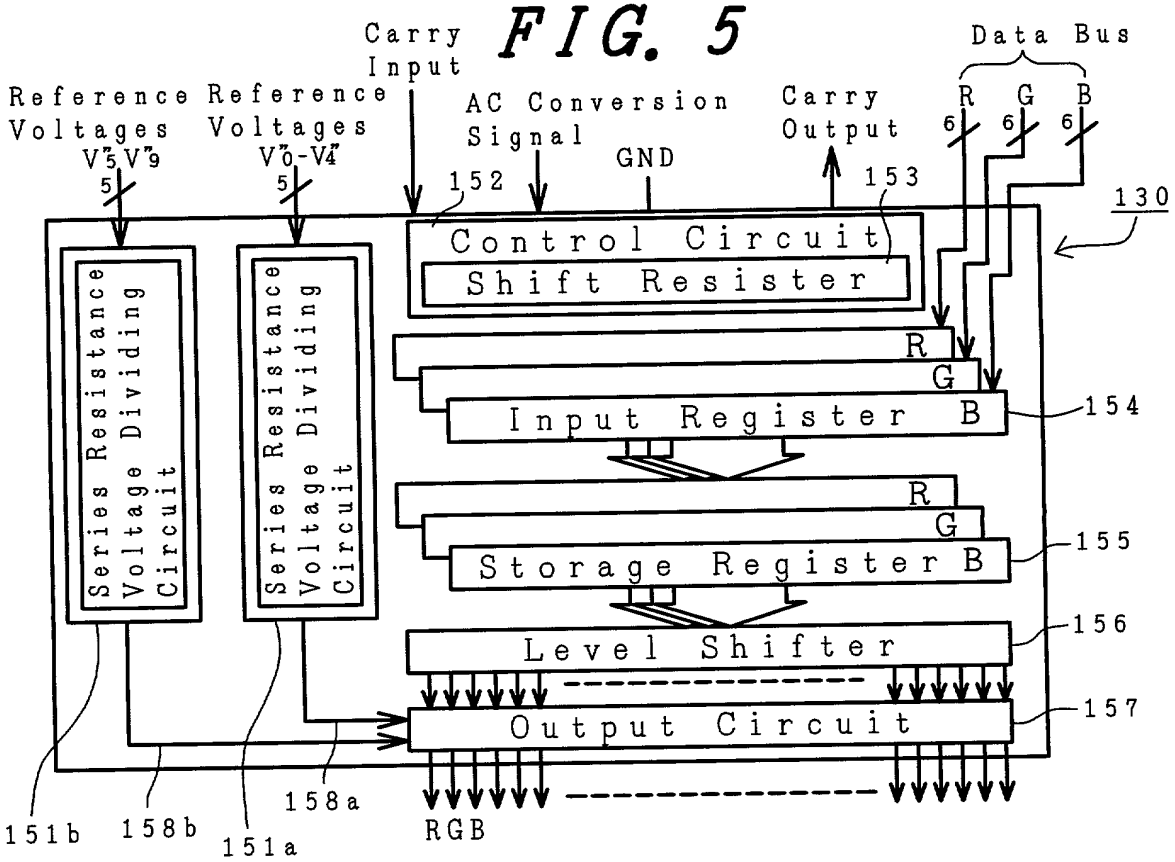

Carry Input
Data Bus
Reference Voltages V"5 V"9
Reference Voltages V"0-V"4
AC Conversion Signal
GND
Carry Output
R G B
6 6 6
152
153
130
Control Circuit
Shift Resister
Input Register B
Storage Register B
Level Shifter
Output Circuit
Series Resistance Voltage Dividing Circuit
154
155
156
157
151b
158b
151a
158a
RGB

FIG. 6

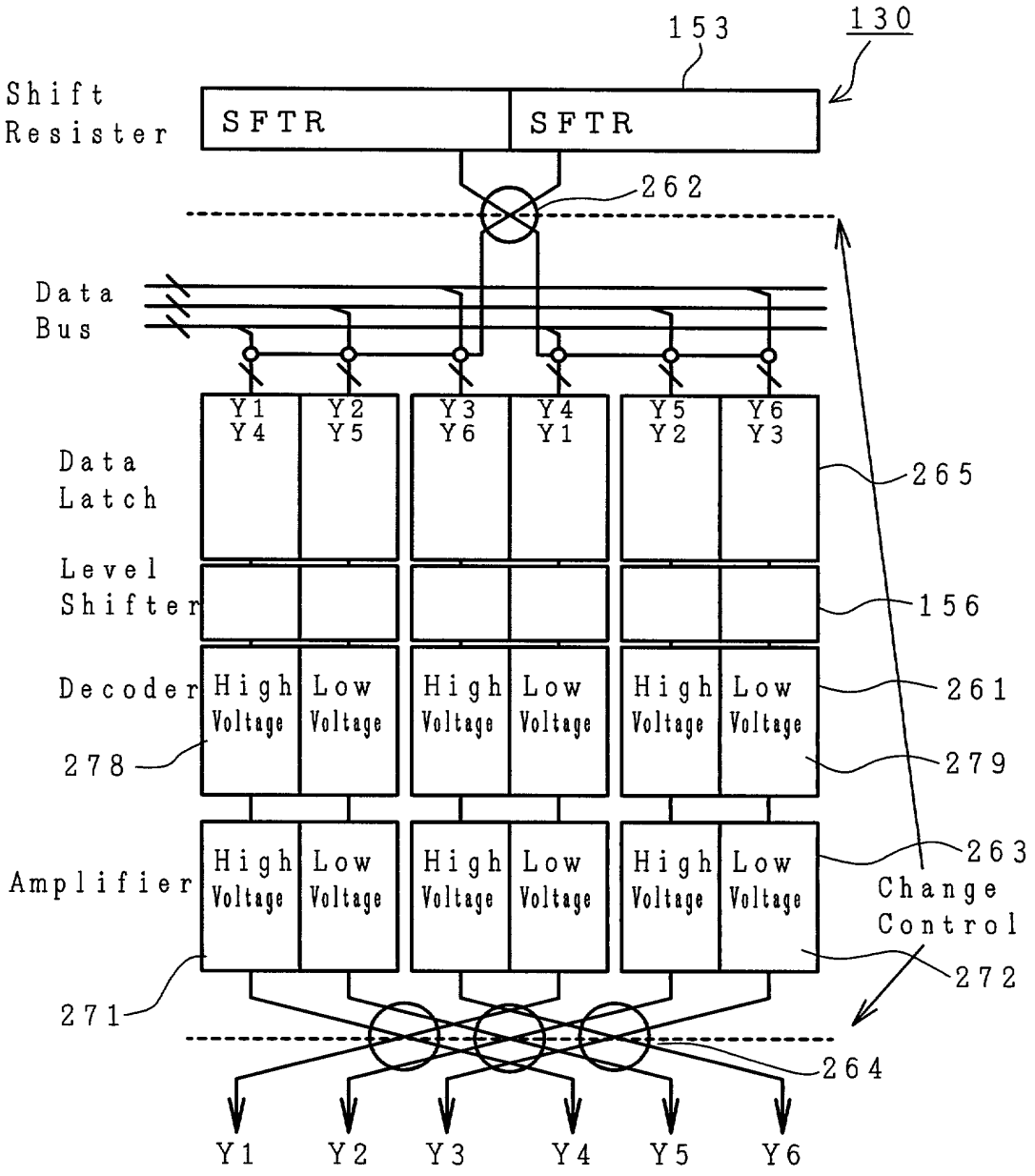

153
130
Shift Resister
SFTR
SFTR
262
Data Bus
Y1 Y4
Y2 Y5
Y3 Y6
Y4 Y1
Y5 Y2
Y6 Y3
Data Latch
265
Level Shifter
156
Decoder
High Voltage
Low Voltage
261
278
279
Amplifier
263
Change Control
272
271
264
Y1
Y2
Y3
Y4
Y5
Y6

FIG. 7

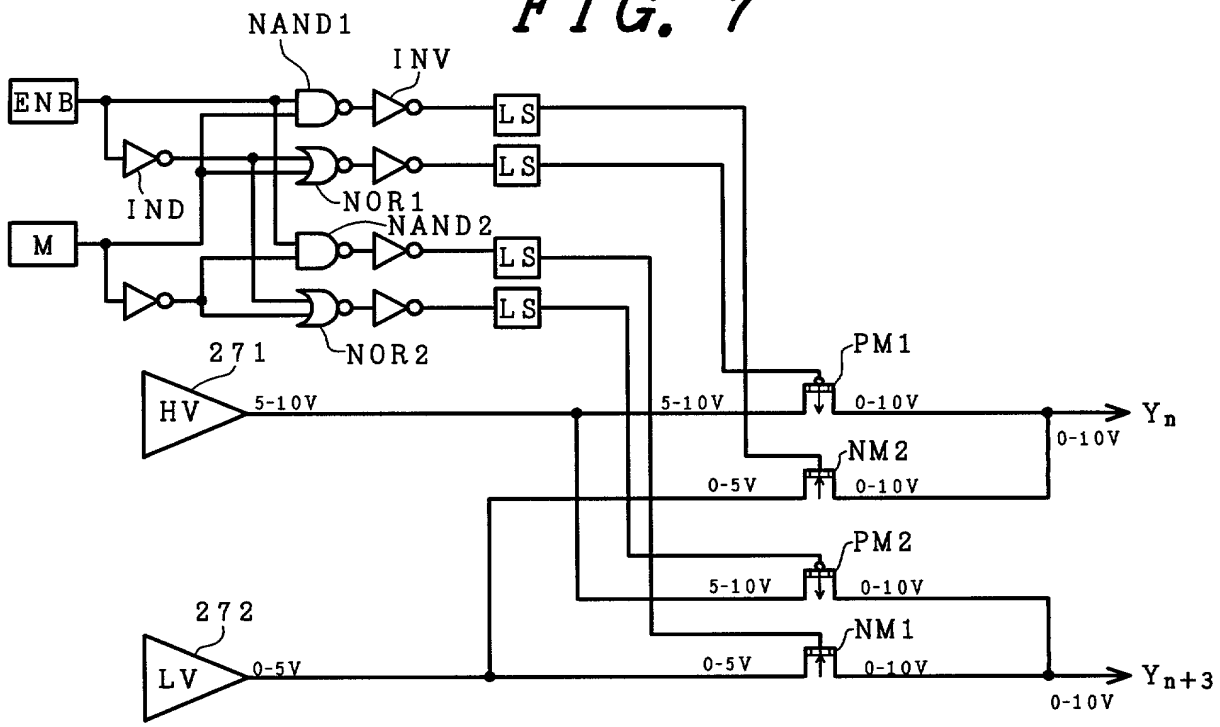

NAND1
INV
ENB
LS
LS
IND
NOR1
NAND2
M
LS
LS
NOR2
271
PM1
HV
5-10V
5-10V
0-10V
Yn
0-10V
NM2
0-5V
0-10V
PM2
5-10V
0-10V
272
NM1
LV
0-5V
0-5V
0-10V
Yn+3
0-10V

FIG. 8

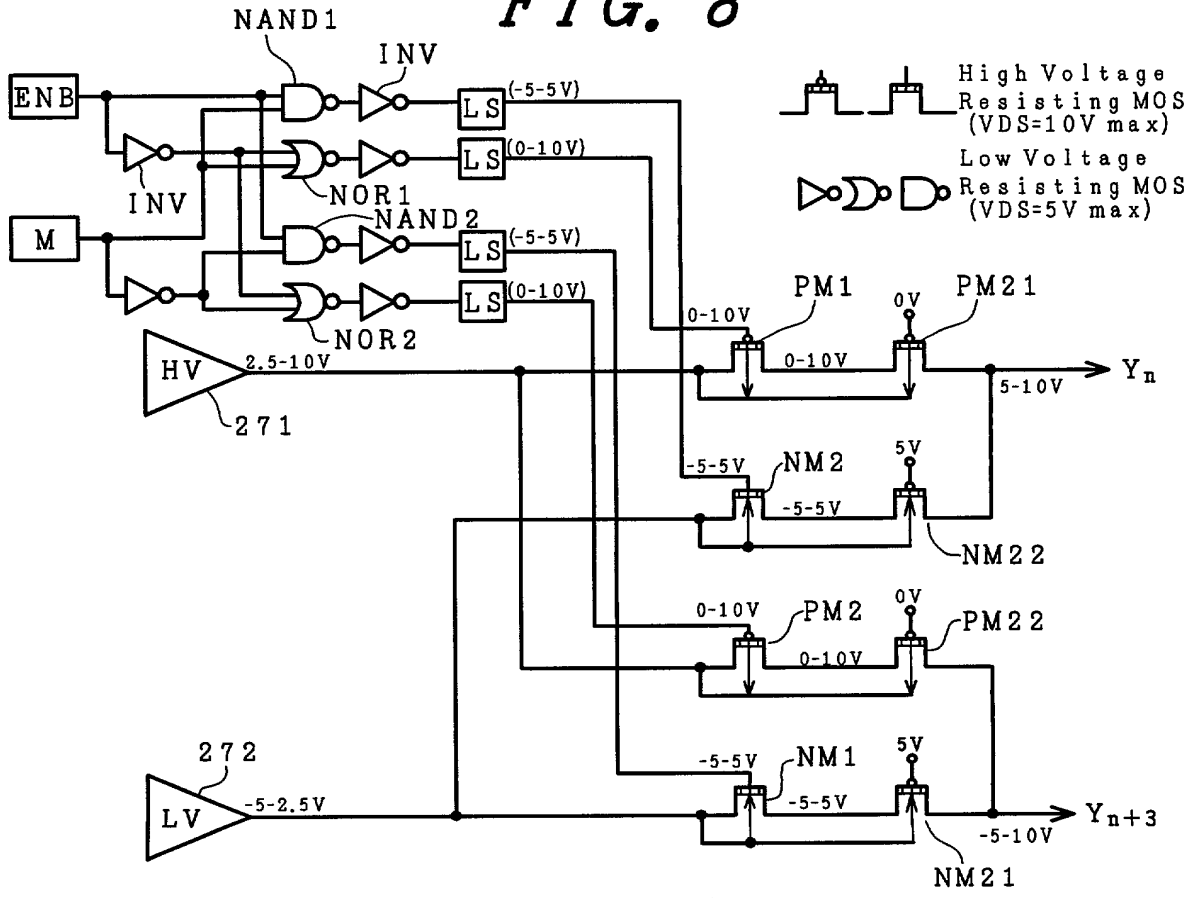

NAND1
INV
ENB
(-5-5V)
LS
(0-10V)
LS
INV
NOR1
NAND2
M
LS
(-5-5V)
LS
(0-10V)
NOR2
High Voltage Resisting MOS (VDS=10V max)
Low Voltage Resisting MOS (VDS=5V max)
PM1
0V
PM21
0-10V
HV
2.5-10V
0-10V
Yn
271
5-10V
-5-5V
NM2
5V
-5-5V
NM22
0-10V
PM2
0V
PM22
0-10V
272
-5-5V
NM1
5V
LV
-5-2.5V
-5-5V
Yn+3
-5-10V
NM21

FIG. 9

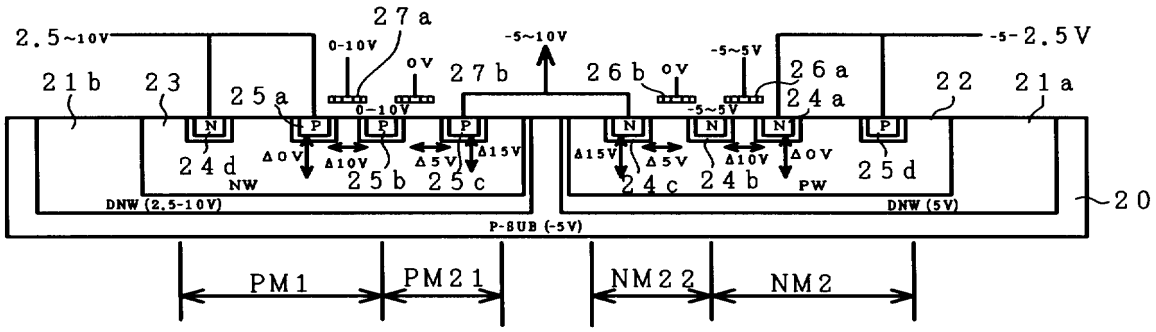

2.5~10V
27a
0-10V
0V
-5~10V
-5~5V
-5~2.5V
21b
23
25a
27b
26b
0V
26a
24a
22
21a
0-10V
-5~5V
24d
NW
ΔOV
Δ10V
Δ5V
Δ15V
25b
25c
Δ15V
Δ5V
24c
24b
Δ10V
ΔOV
PW
25d
DNW (2.5-10V)
DNW (5V)
20
P-SUB (-5V)
PM1
PM21
NM22
NM2

FIG. 10A

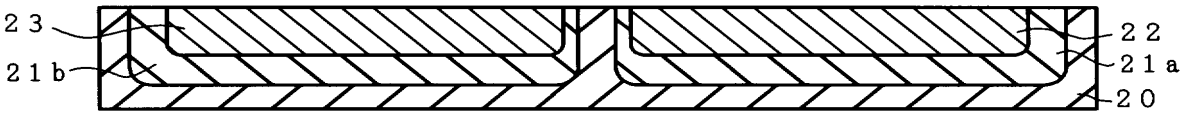


FIG. 10B

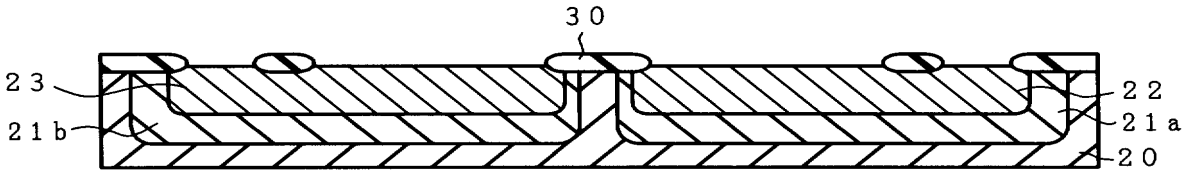


FIG. 10C

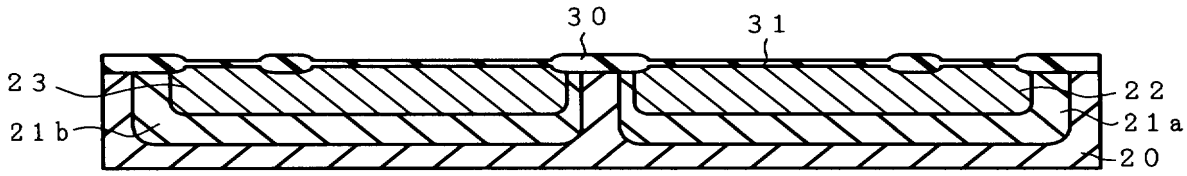


FIG. 10D

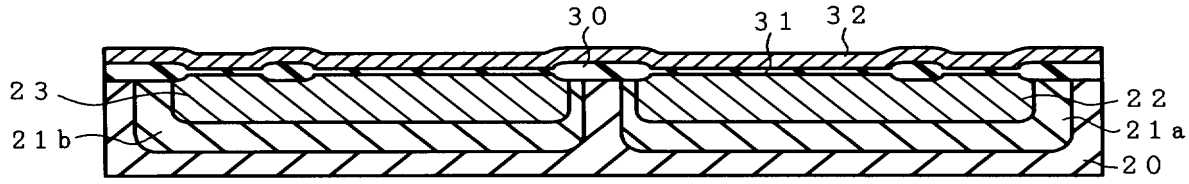


FIG. 10E

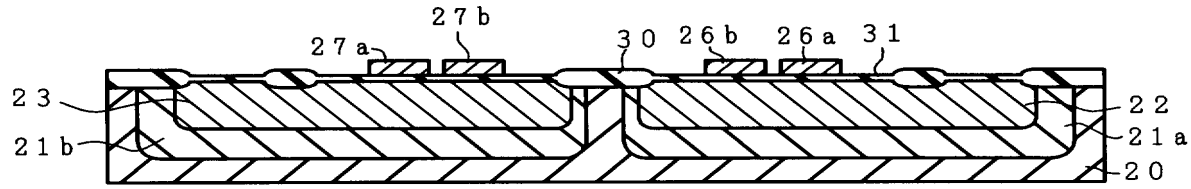


FIG. 11A

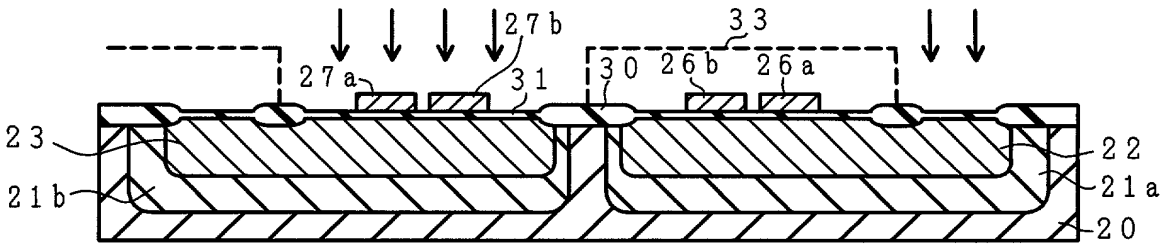


FIG. 11B

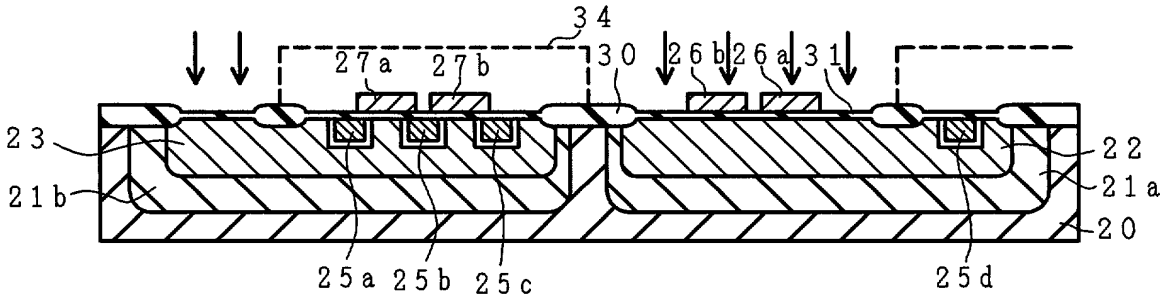


FIG. 11C

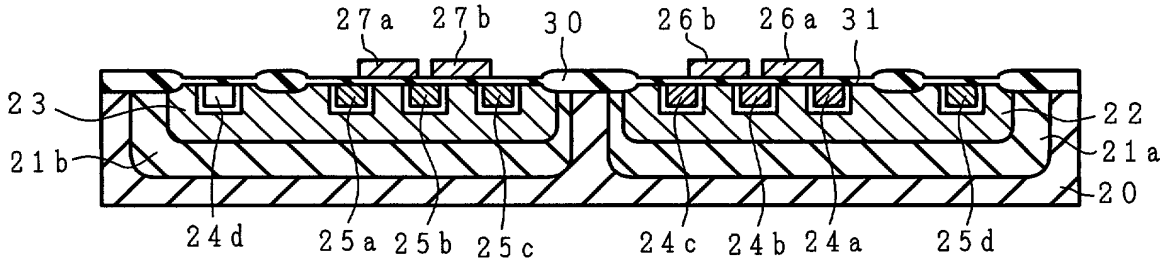


FIG. 11D

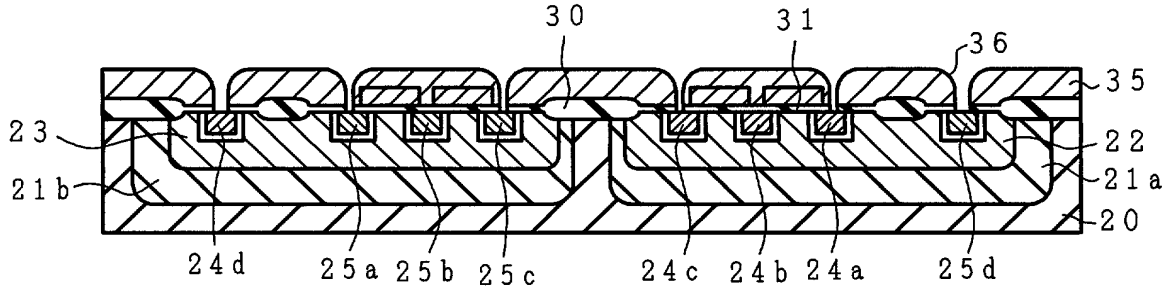


FIG. 11E

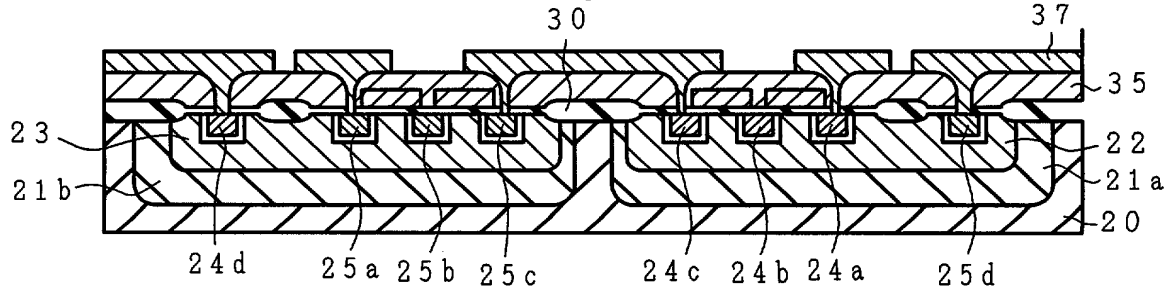


FIG. 12

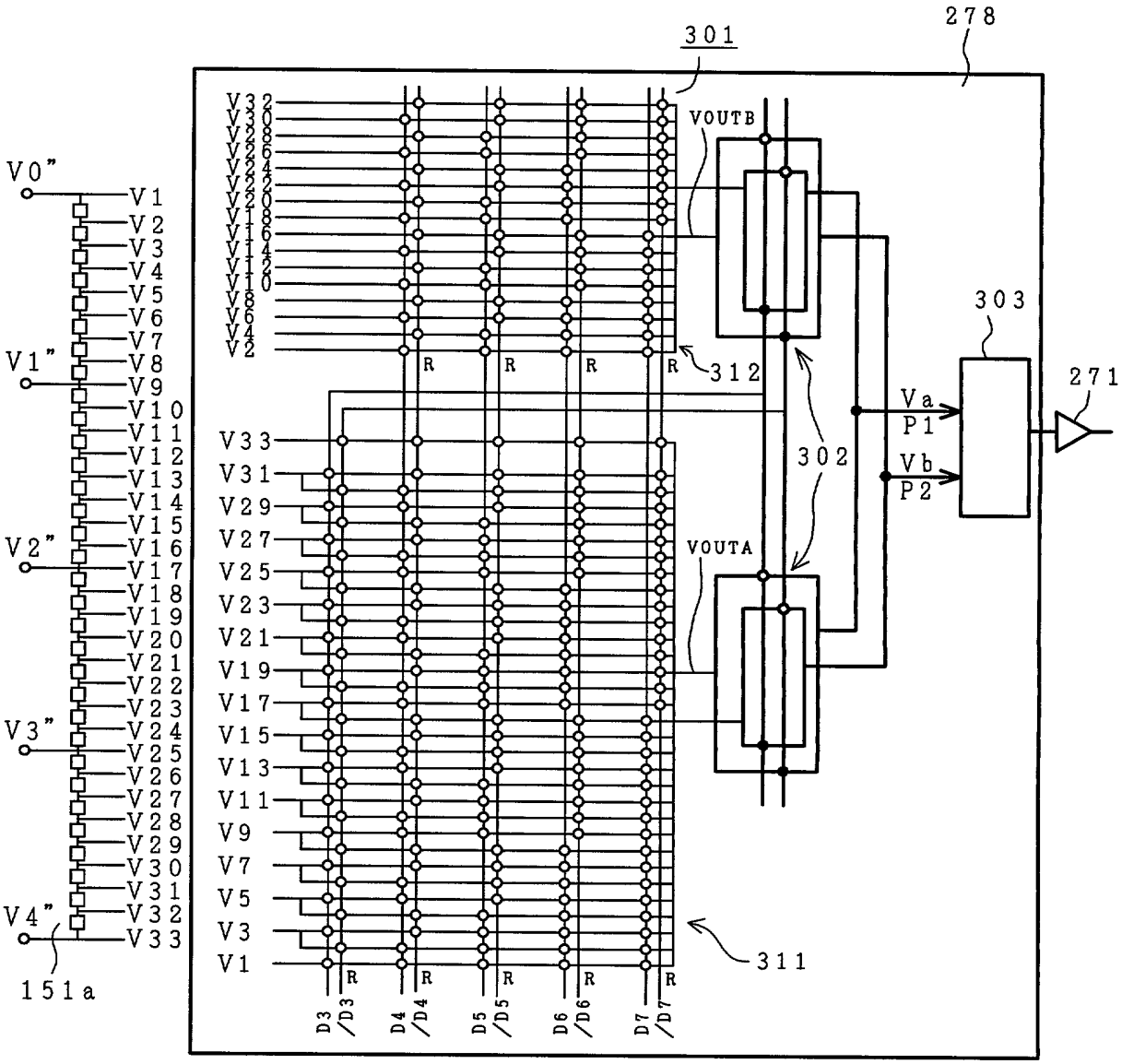

278
301
V0"
V1"
V2"
V3"
V4"
151a
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
V11
V12
V13
V14
V15
V16
V17
V18
V19
V20
V21
V22
V23
V24
V25
V26
V27
V28
V29
V30
V31
V32
V33
VOUTB
VOUTA
312
311
302
303
271
Va
P1
Vb
P2
R
D3
/D3
D4
/D4
D5
/D5
D6
/D6
D7
/D7

FIG. 13

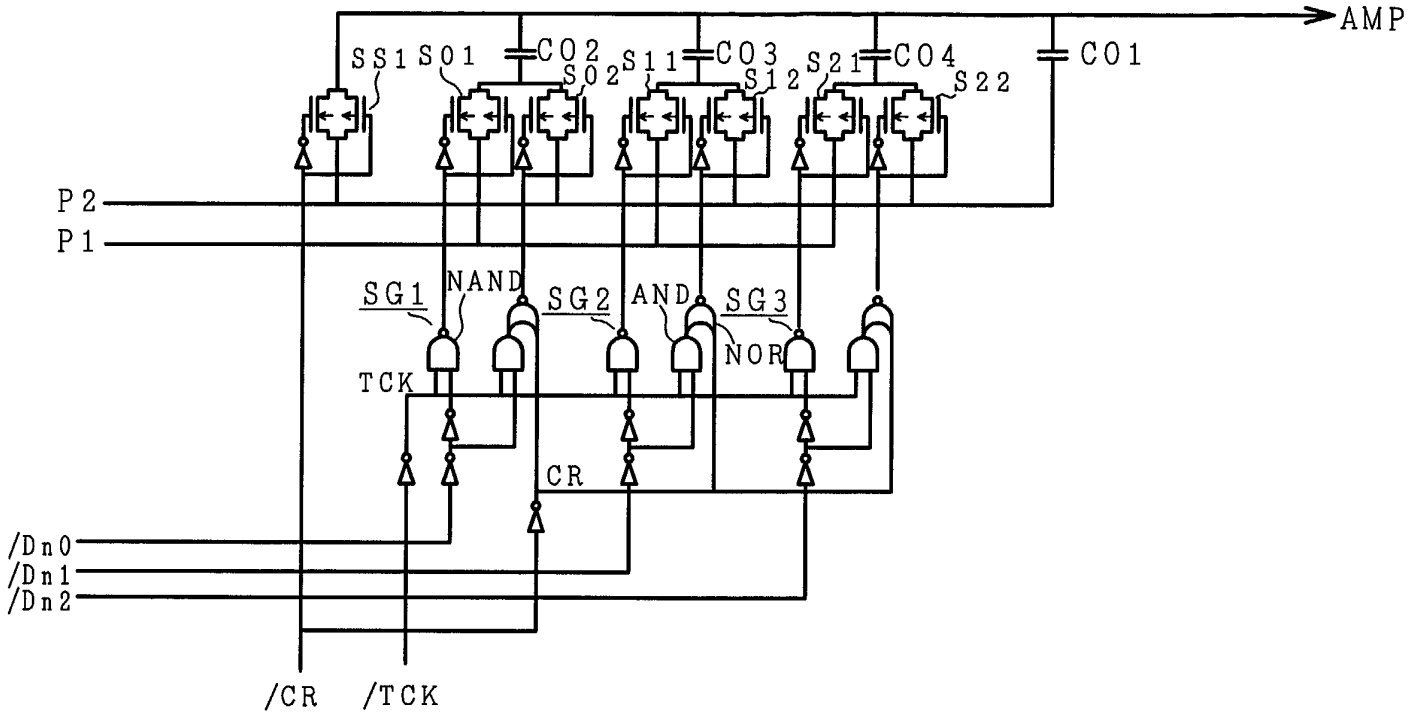


FIG. 14

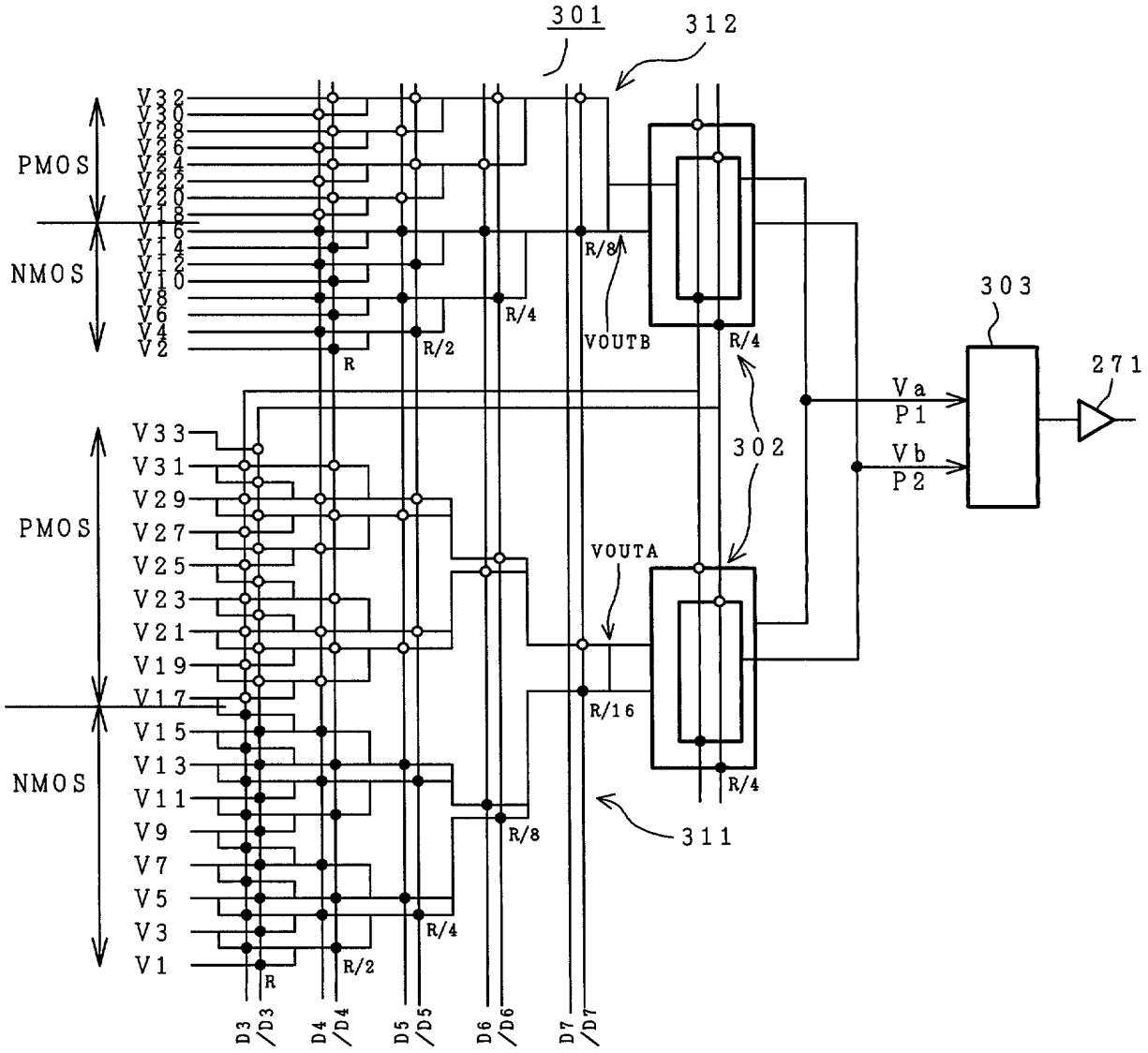

301
312
PMOS
NMOS
V32
V30
V28
V26
V24
V22
V20
V18
V16
V14
V12
V10
V8
V6
V4
V2
R
R/2
R/4
R/8
VOUTB
R/4
303
271
Va
P1
Vb
P2
302
PMOS
NMOS
V33
V31
V29
V27
V25
V23
V21
V19
V17
V15
V13
V11
V9
V7
V5
V3
V1
VOUTA
R/16
R/4
311
R/8
R/4
R/2
R
D3
/D3
D4
/D4
D5
/D5
D6
/D6
D7
/D7

FIG. 15

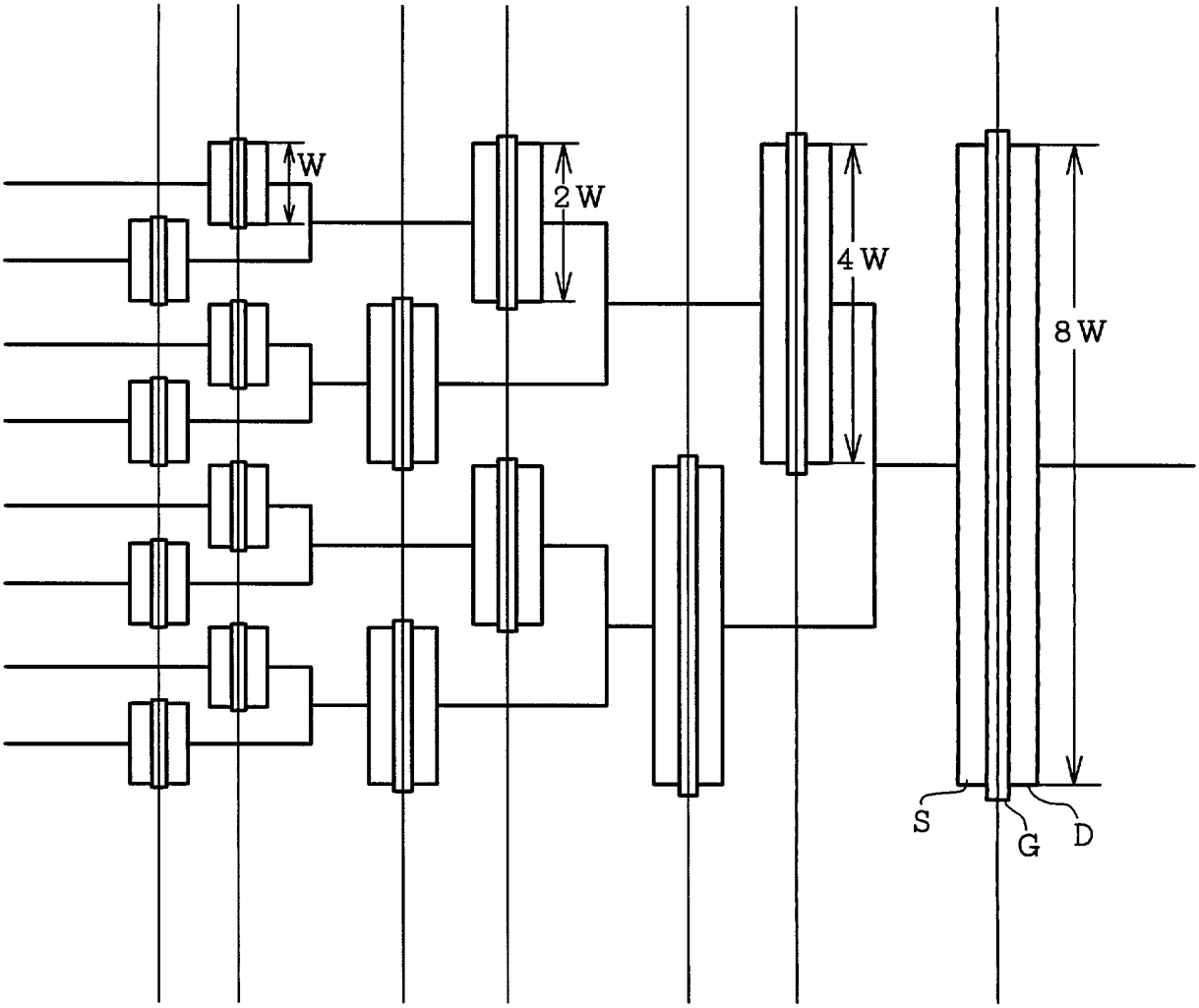


FIG. 16

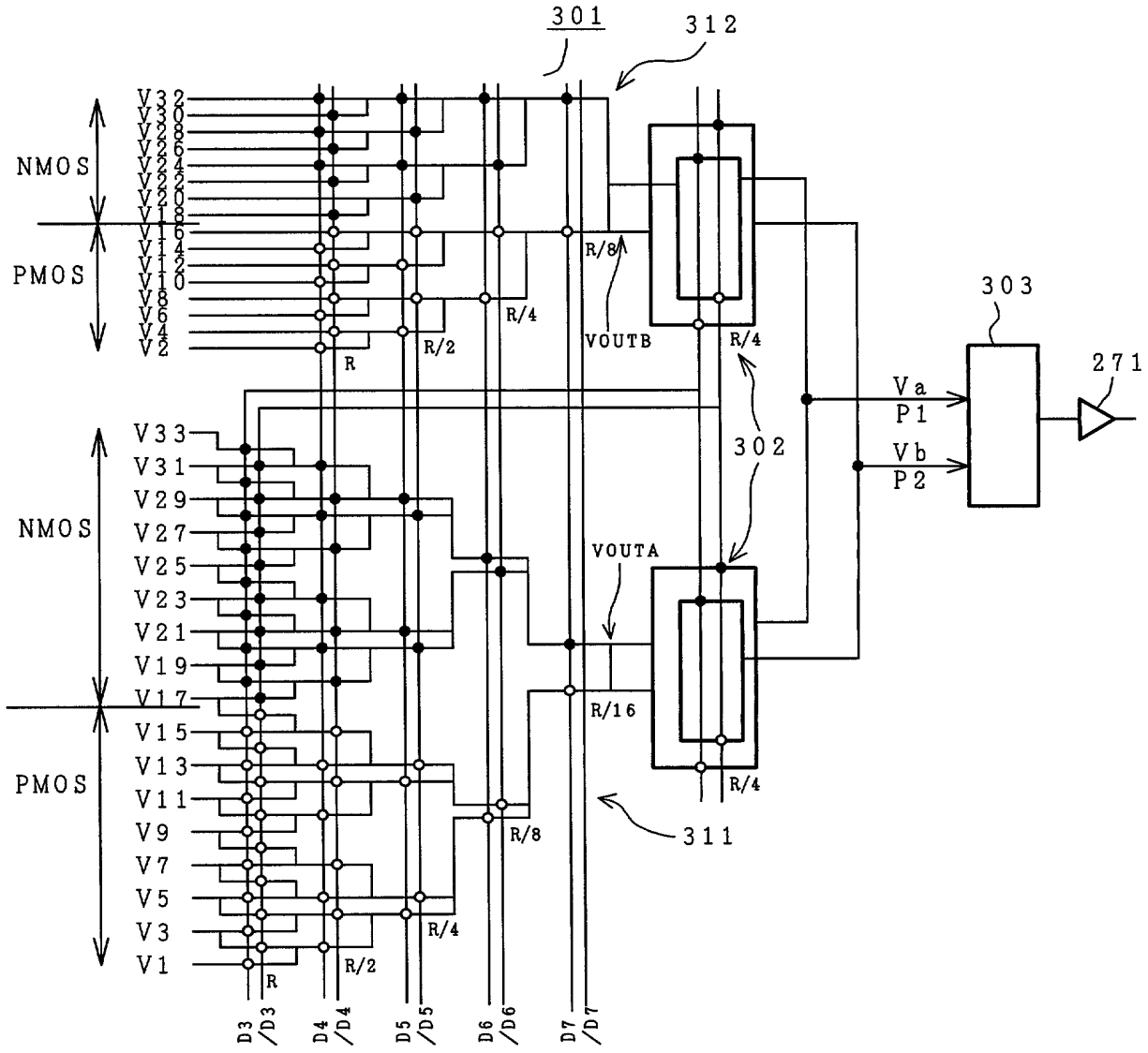

301
312
NMOS
PMOS
V32
V30
V28
V26
V24
V22
V20
V18
V16
V14
V12
V10
V8
V6
V4
V2
R
R/2
R/4
R/8
VOUTB
R/4
303
271
Va
P1
Vb
P2
302
NMOS
PMOS
V33
V31
V29
V27
V25
V23
V21
V19
V17
V15
V13
V11
V9
V7
V5
V3
V1
VOUTA
R/16
R/4
311
R/8
R/4
R/2
R
D3
/D3
D4
/D4
D5
/D5
D6
/D6
D7
/D7

FIG. 17

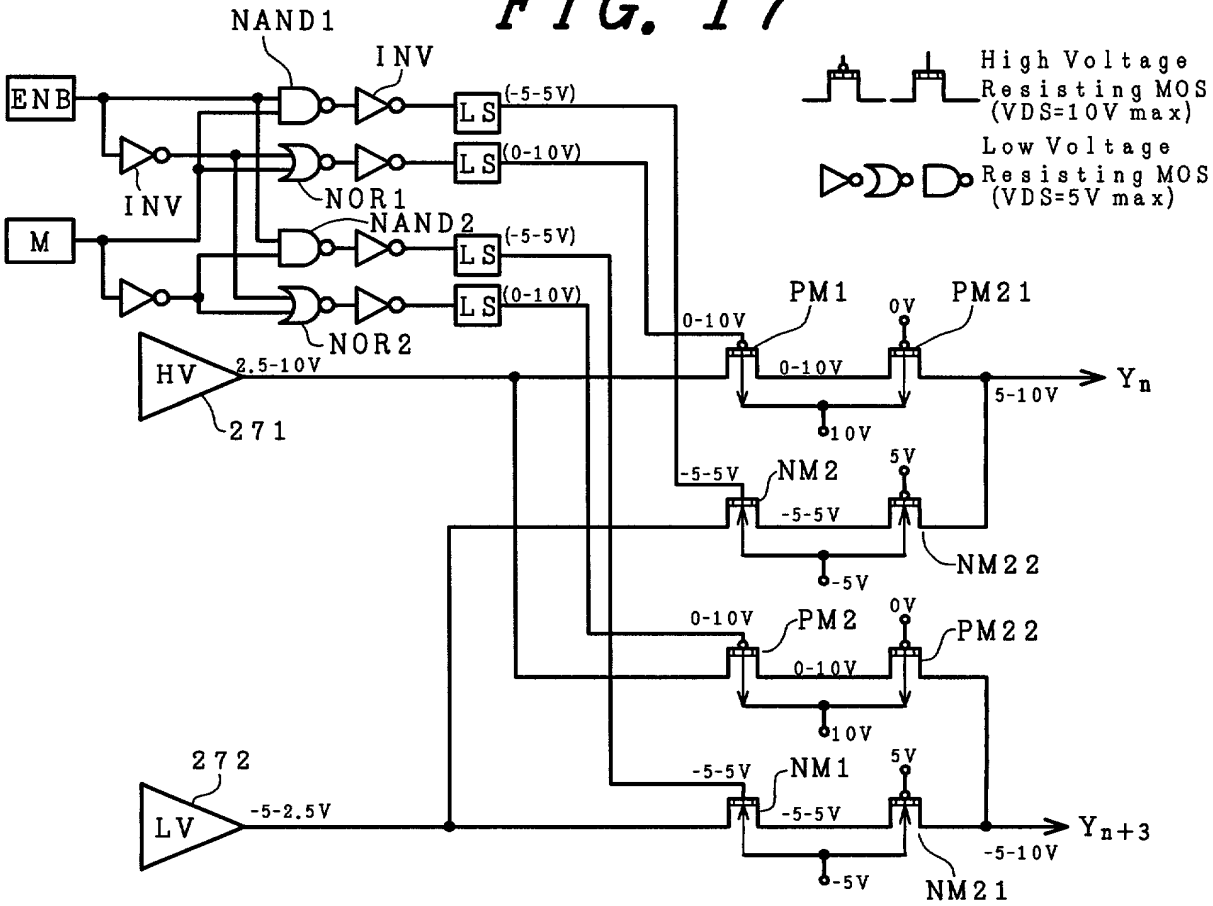

NAND1
INV
ENB
LS
(-5-5V)
(0-10V)
INV
NOR1
NAND2
M
NOR2
HV
2.5-10V
271
High Voltage Resisting MOS (VDS=10V max)
Low Voltage Resisting MOS (VDS=5V max)
PM1
PM21
0V
0-10V
10V
Yn
5-10V
-5-5V
NM2
5V
NM22
-5V
PM2
PM22
272
LV
-5-2.5V
NM1
Yn+3
-5-10V
NM21

FIG. 18

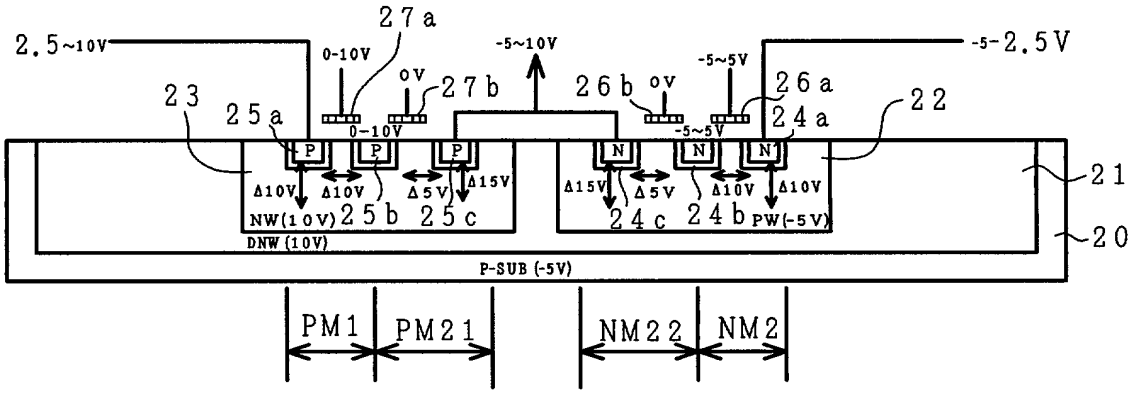

2.5~10V
27a
0-10V
-5~10V
-5~5V
-5~2.5V
23
25a
27b
26b
0V
26a
24a
22
Δ10V
Δ5V
Δ15V
NW(10V)
25b
25c
24c
24b
PW(-5V)
DNW(10V)
P-SUB (-5V)
21
20
PM1
PM21
NM22
NM2

FIG. 19

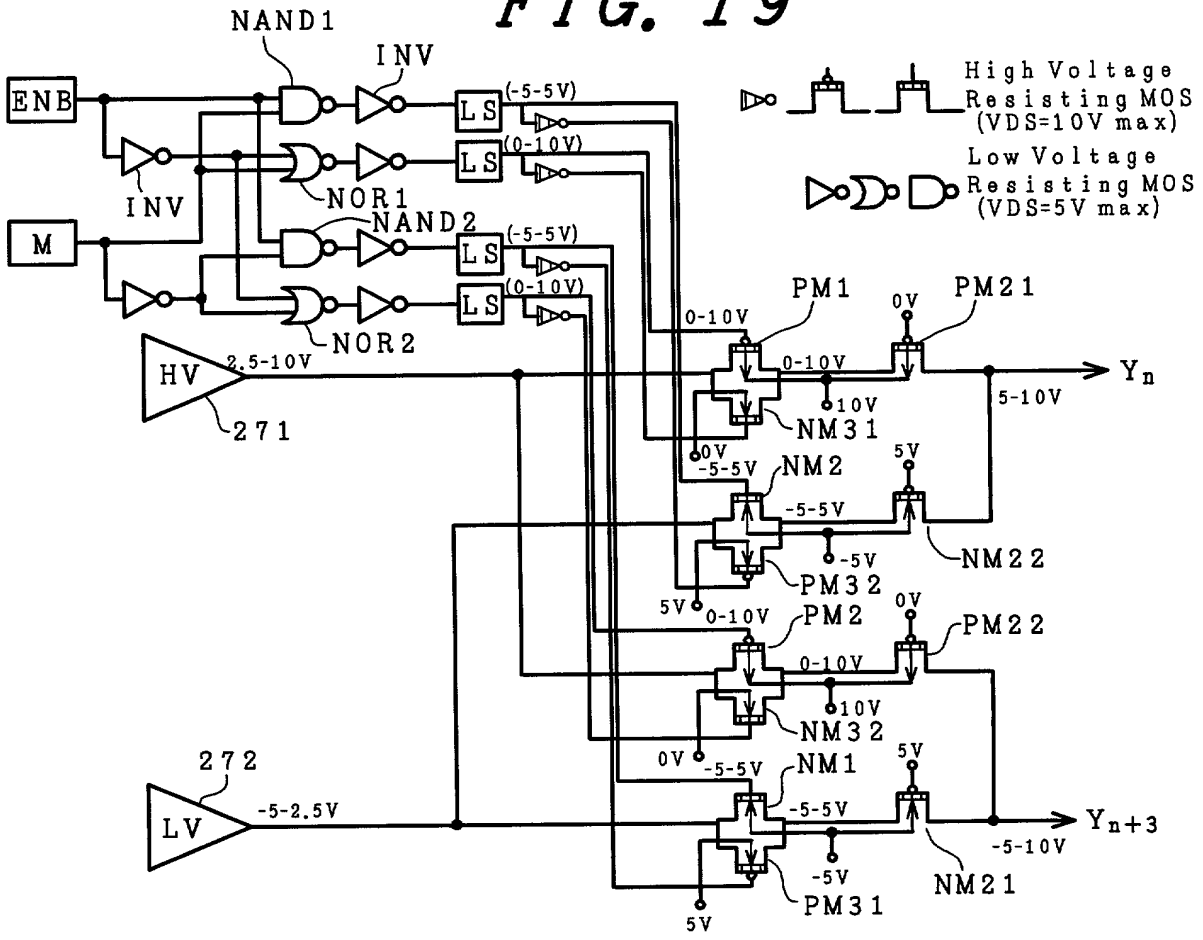

NAND1
INV
ENB
INV
M
NOR1
NAND2
NOR2
LS
(-5-5V)
(0-10V)
High Voltage Resisting MOS (VDS=10V max)
Low Voltage Resisting MOS (VDS=5V max)
HV
2.5-10V
271
LV
272
-5-2.5V
PM1
PM21
PM31
PM32
PM2
PM22
NM1
NM21
NM31
NM32
NM2
NM22
0V
5V
-5V
0-10V
5-10V
-5-5V
Yn
Yn+3

FIG. 20

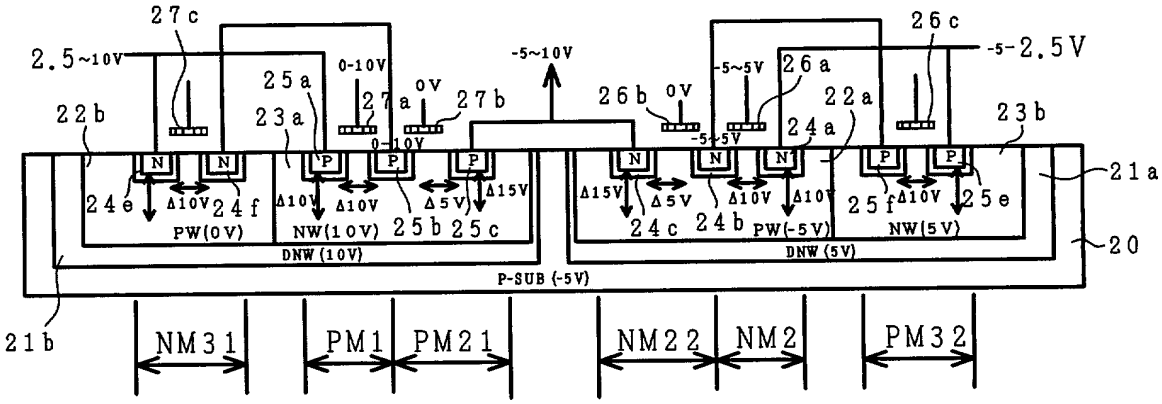

27c
26c
2.5~10V
-5~10V
-5-2.5V
25a
27a
27b
26b
26a
22a
22b
23a
23b
24a
24e
24f
24b
24c
25b
25c
25e
25f
21a
20
21b
PW(0V)
NW(10V)
PW(-5V)
NW(5V)
DNW(10V)
DNW(5V)
P-SUB(-5V)
NM31
PM1
PM21
NM22
NM2
PM32

FIG. 21

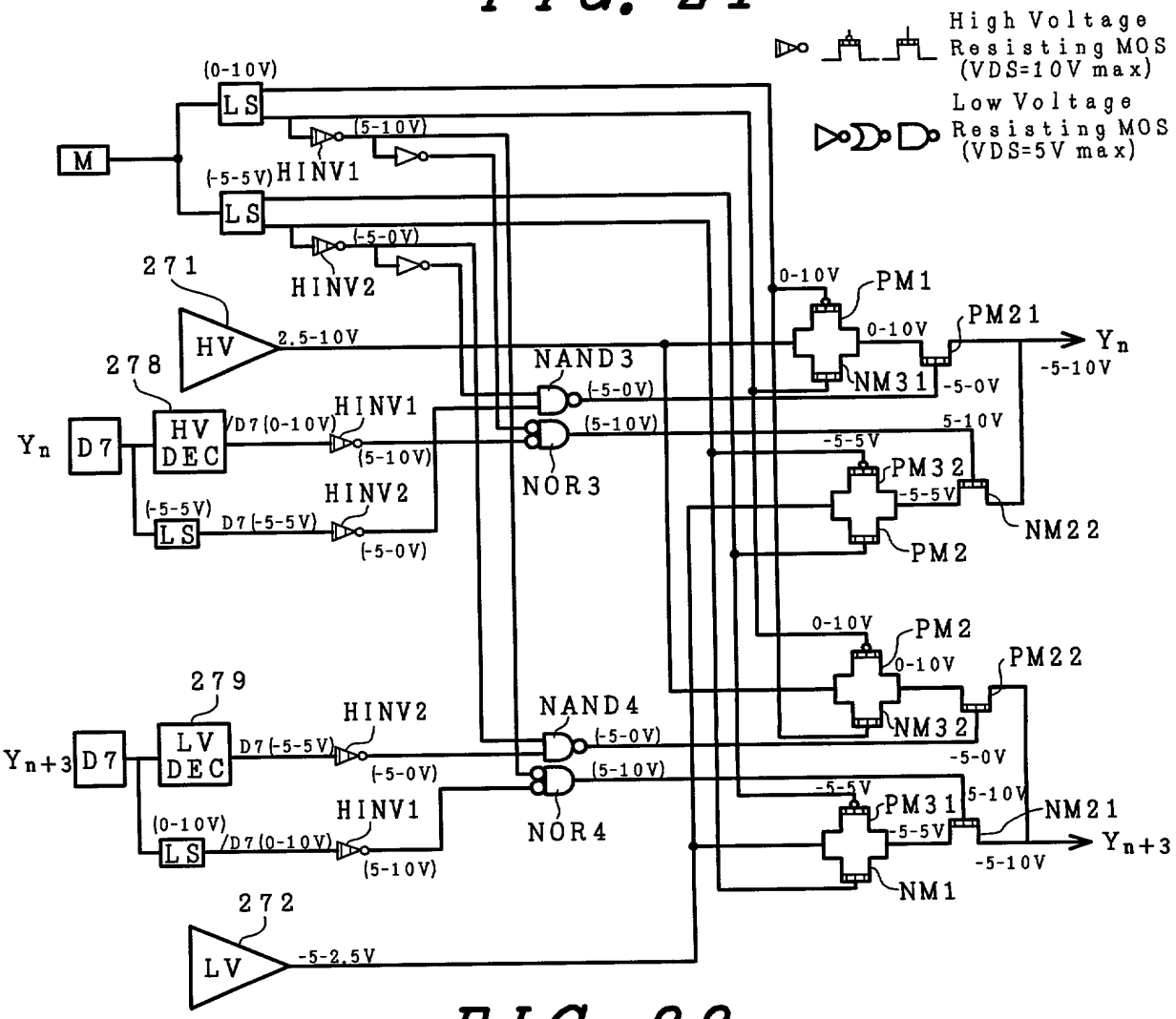

High Voltage Resisting MOS (VDS=10V max)
Low Voltage Resisting MOS (VDS=5V max)
M
LS
(0-10V)
(5-10V)
HINV1
(-5-5V)
(-5-0V)
HINV2
271
HV
2.5-10V
278
HV DEC
D7(0-10V)
D7(-5-5V)
Yn
D7
NAND3
NOR3
279
LV DEC
NAND4
NOR4
Yn+3
272
LV
-5-2.5V
PM1
PM21
PM32
PM2
PM22
PM31
NM31
NM22
NM32
NM21
NM1
0-10V
-5-0V
5-10V
-5-5V
-5-10V

FIG. 22

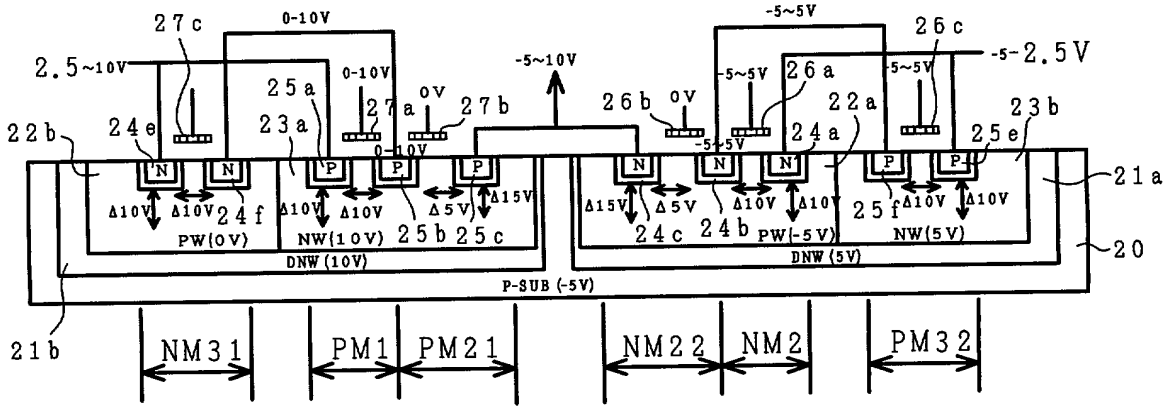

27c
0-10V
2.5~10V
25a
23a
27a
0V
27b
-5~10V
26b
-5~5V
26a
22a
26c
-5-2.5V
22b
24e
24a
23b
25e
21a
Δ10V
Δ5V
Δ15V
24f
PW(0V)
NW(10V)
25b
25c
DNW (10V)
24c
24b
PW(-5V)
25f
NW(5V)
DNW (5V)
20
P-SUB (-5V)
21b
NM31
PM1
PM21
NM22
NM2
PM32

FIG. 23D

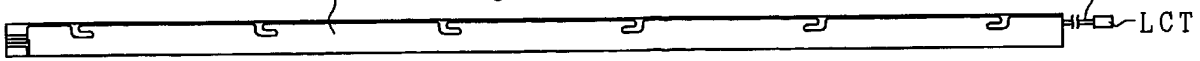


FIG. 23B

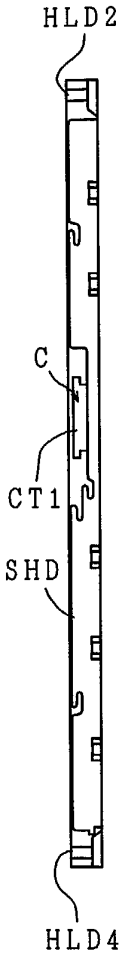


FIG. 23A

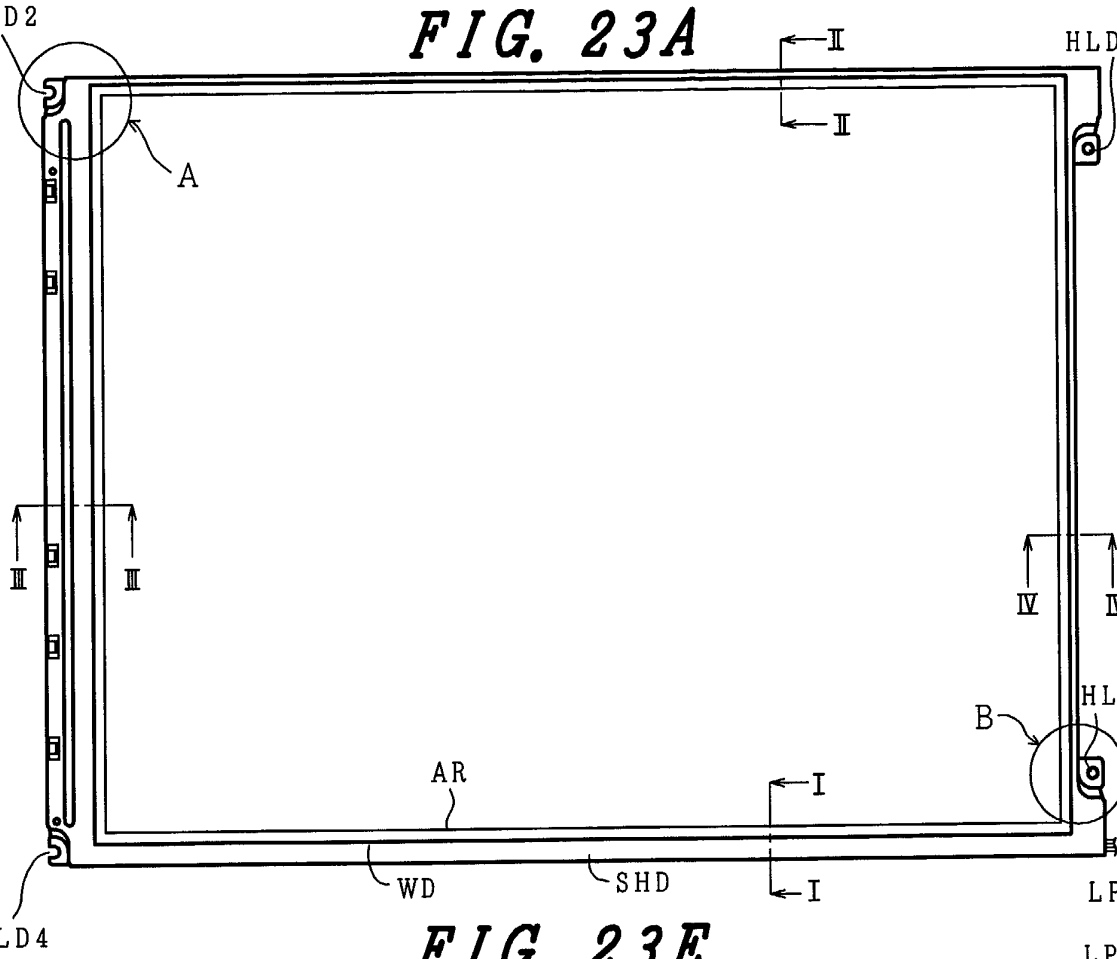


FIG. 23C

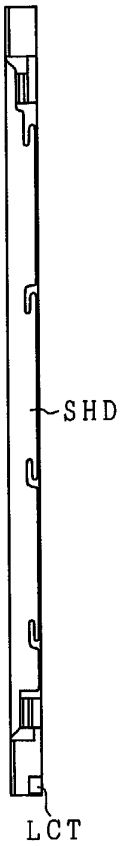


FIG. 23E

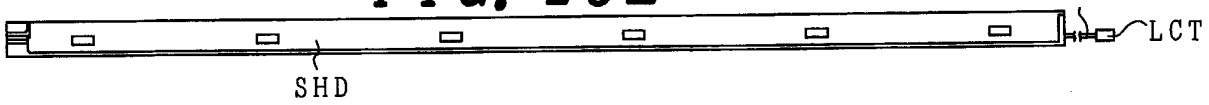


FIG. 24

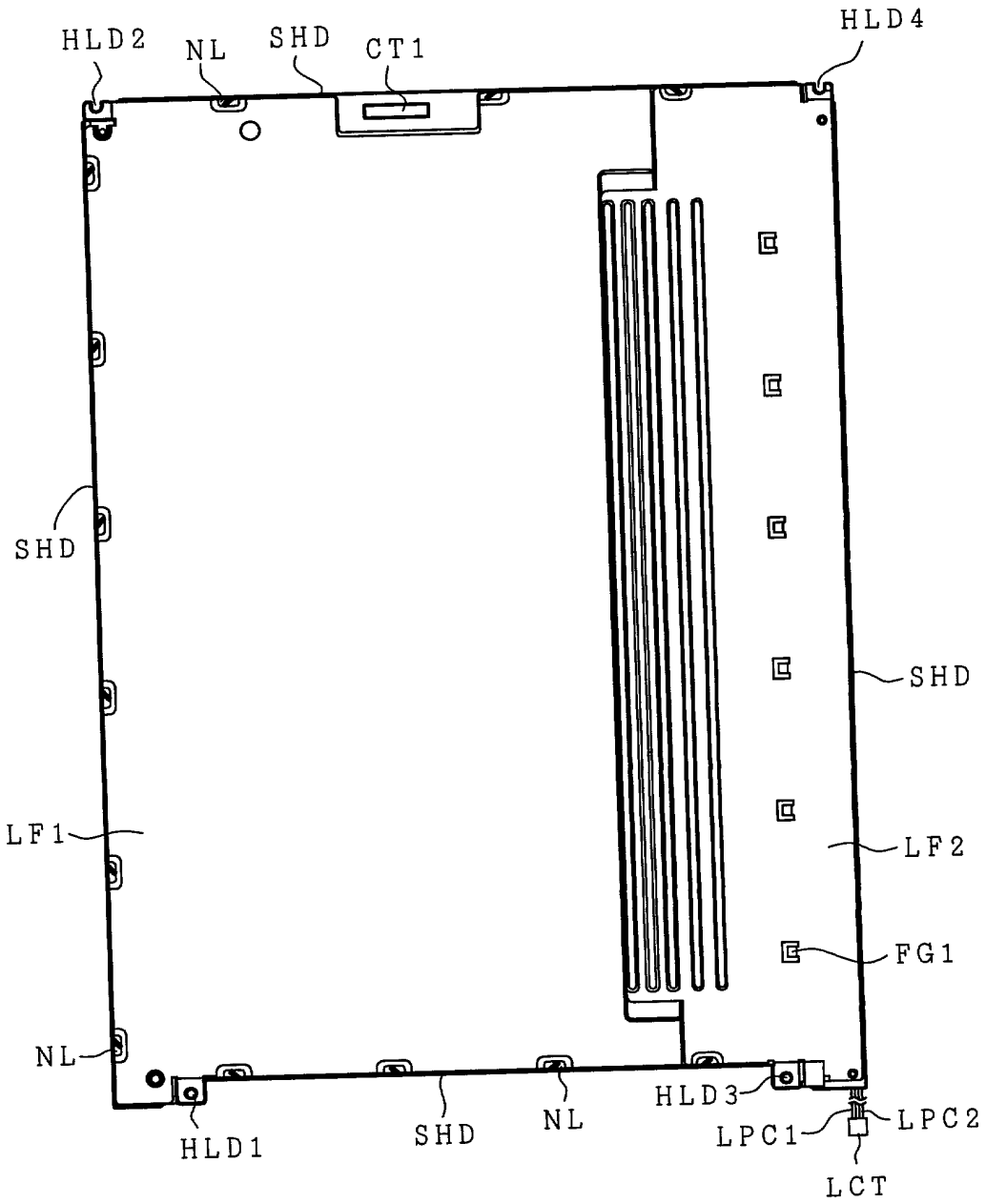

HLD2
NL
SHD
CT1
HLD4
SHD
SHD
LF1
LF2
FG1
NL
HLD1
SHD
NL
HLD3
LPC1
LPC2
LCT

FIG. 25A

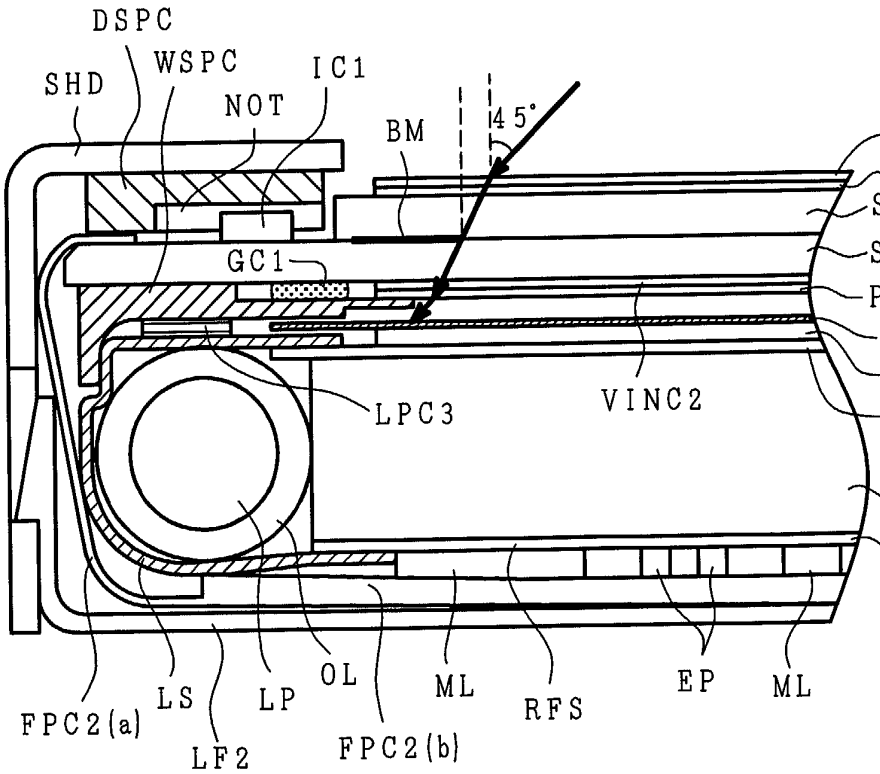


FIG. 25B

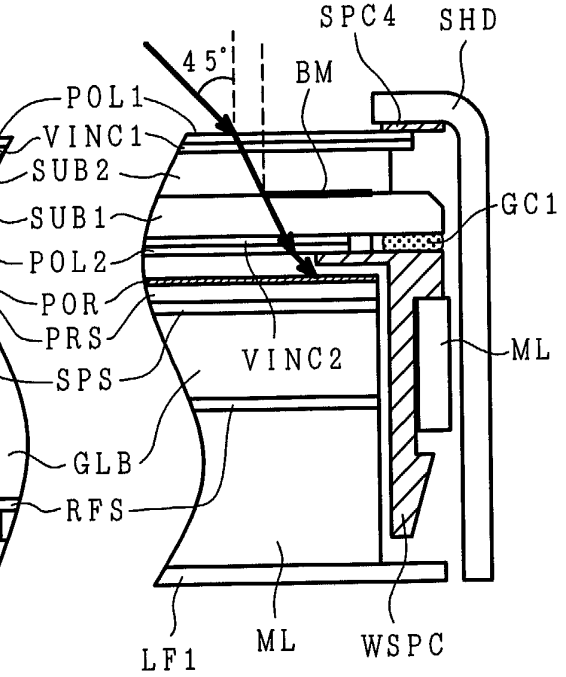
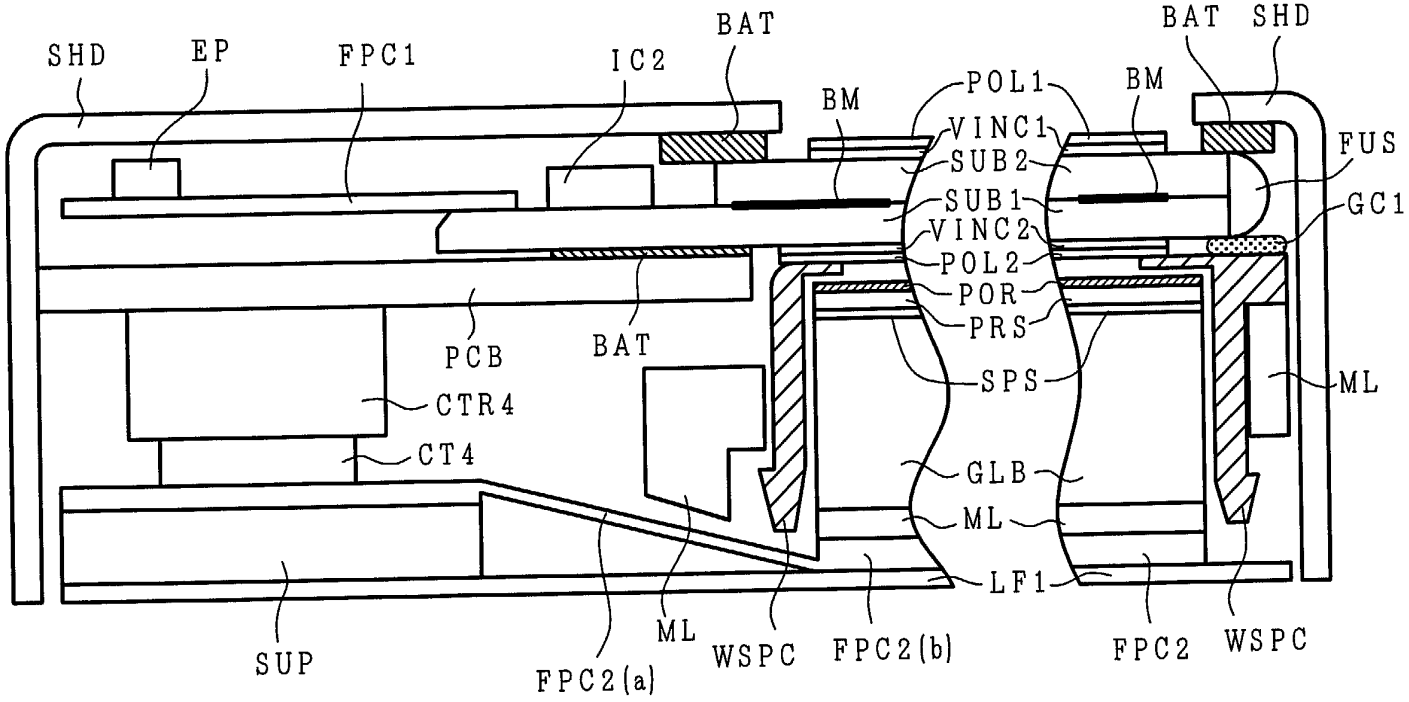


FIG. 26A

FIG. 26B



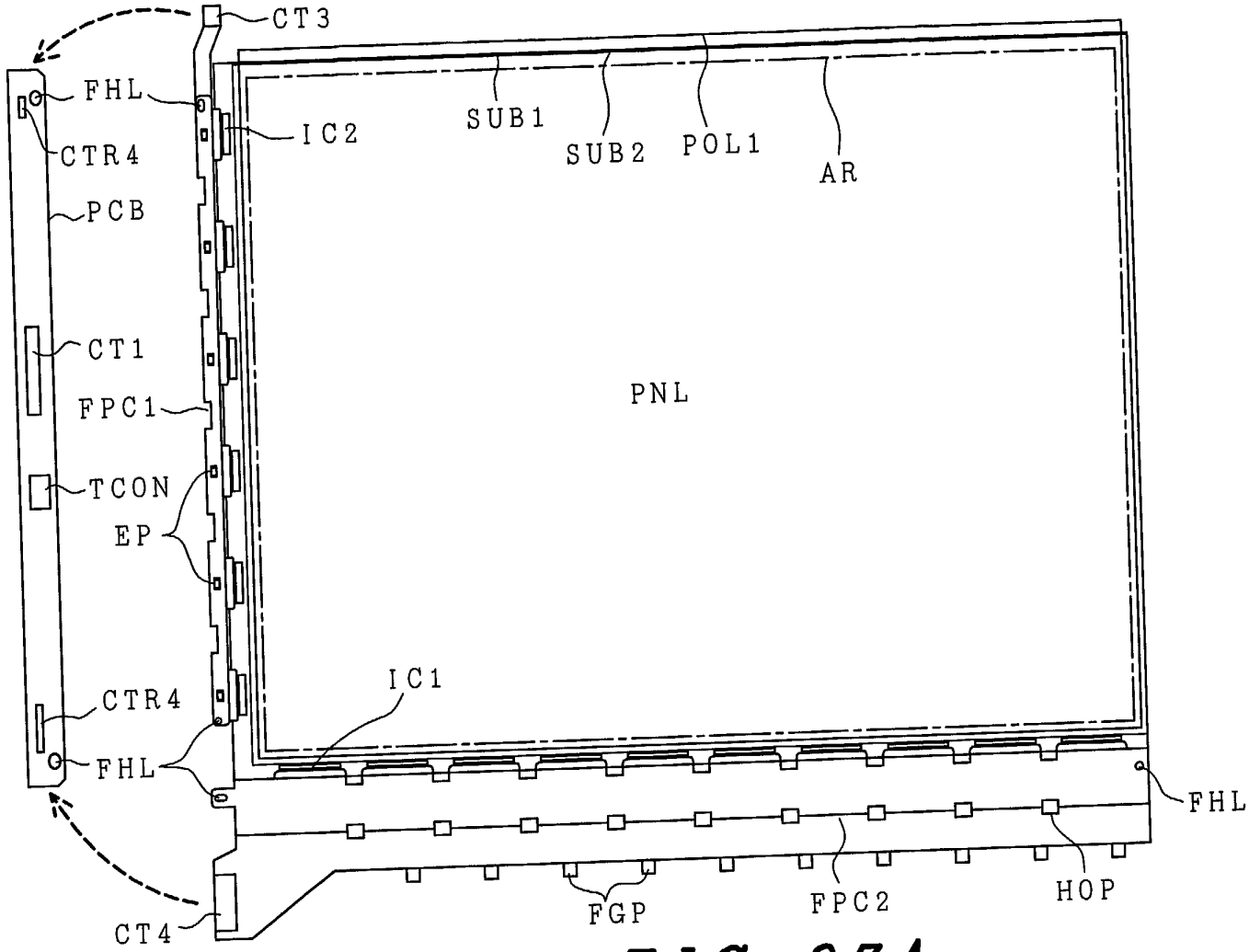


FIG. 27A

FIG. 27B

FIG. 28

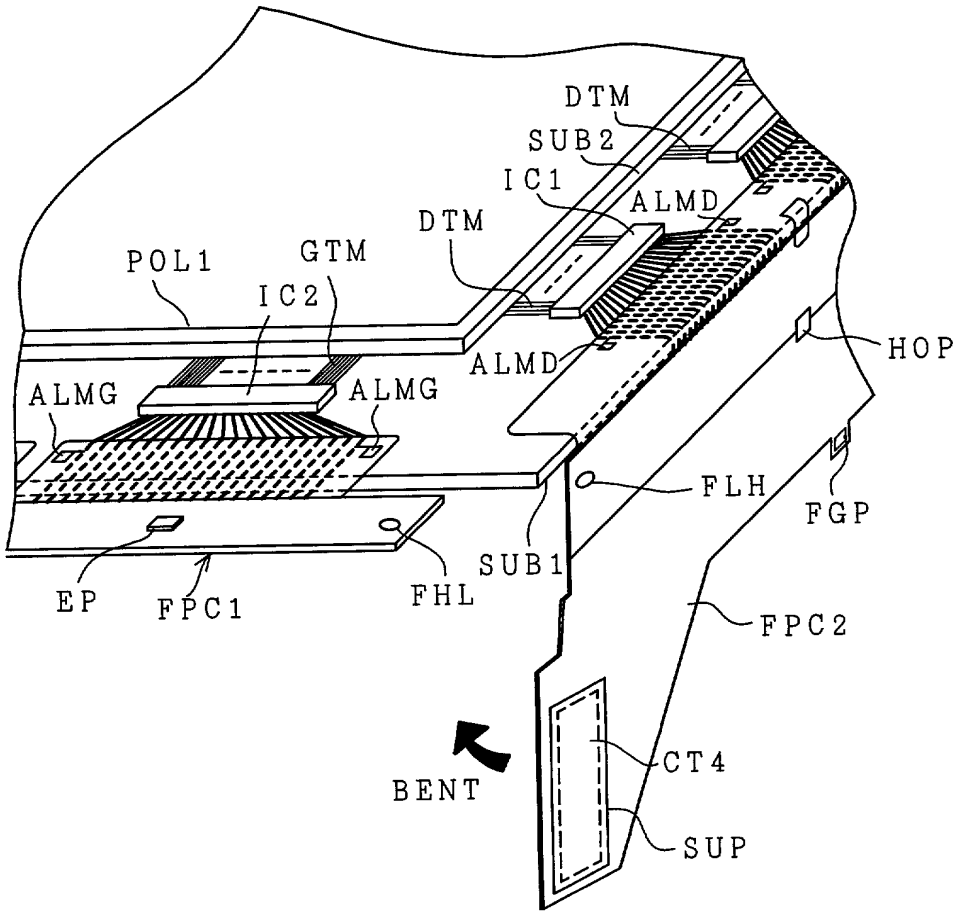

DTM
SUB2
IC1
ALMD
DTM
POL1
GTM
IC2
ALMD
HOP
ALMG
ALMG
FLH
FGP
SUB1
EP
FPC1
FHL
FPC2
BENT
CT4
SUP

FIG. 29

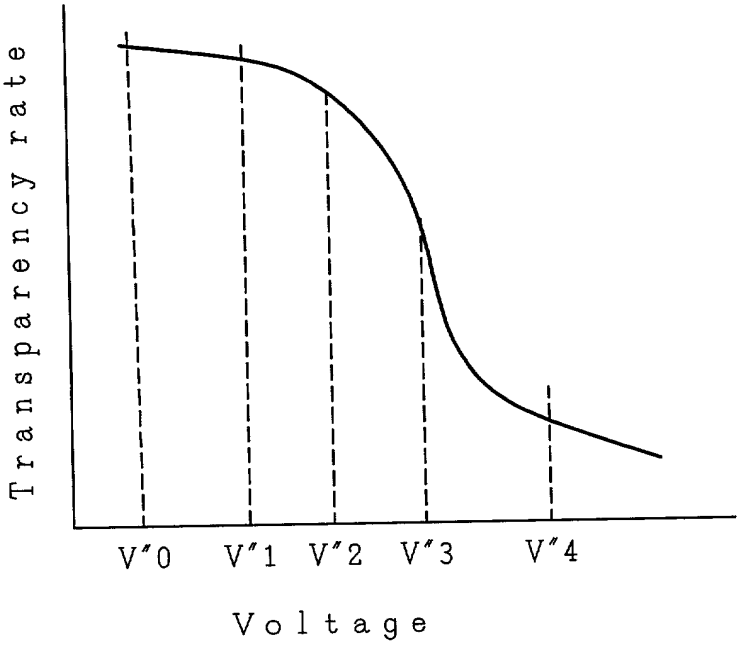
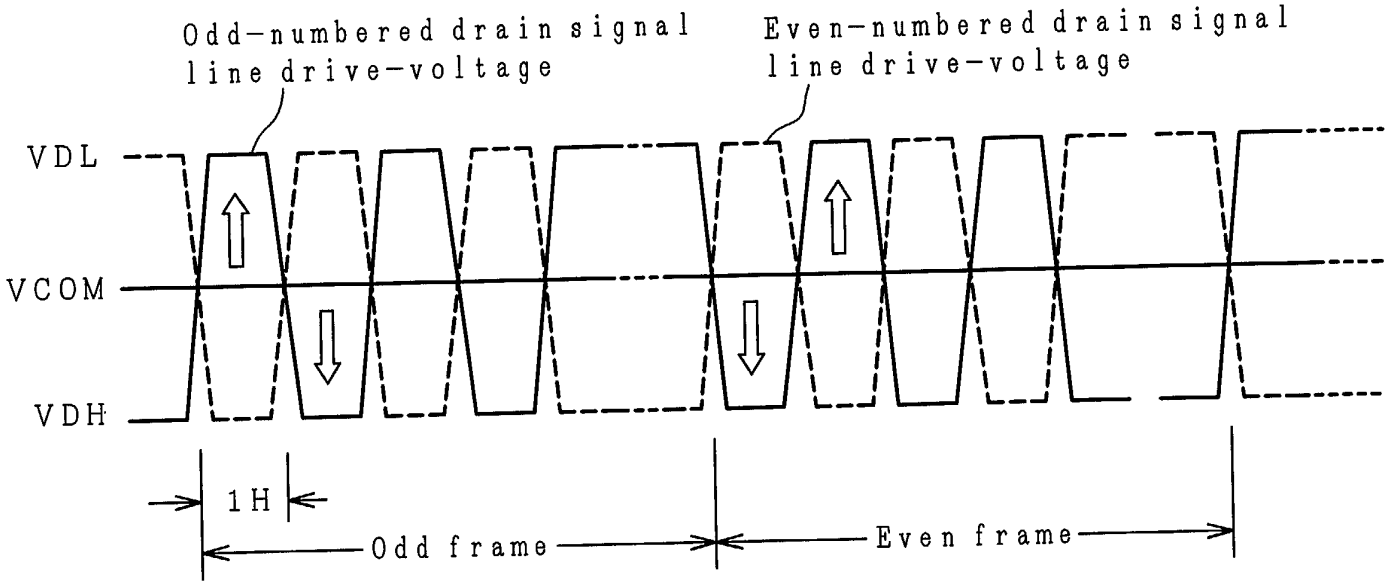

Transparency rate
V″0
V″1
V″2
V″3
V″4
Voltage

FIG. 30


Odd-numbered drain signal line drive-voltage
Even-numbered drain signal line drive-voltage
VDL
VCOM
VDH
1H
Odd frame
Even frame

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, I believe I am original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

LIQUID CRYSTAL DISPLAY DEVICE

the specification of which: (check one) [X] is attached hereto.

[ ] was filed on ____________________

as Application Serial No. ____________________

and was amended on ____________________ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
9-298227 (Number)	Japan (Country)	30th October 1997 (Day/Month/Year Filed)	[X] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application·

(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

(Continued on Page 2)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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